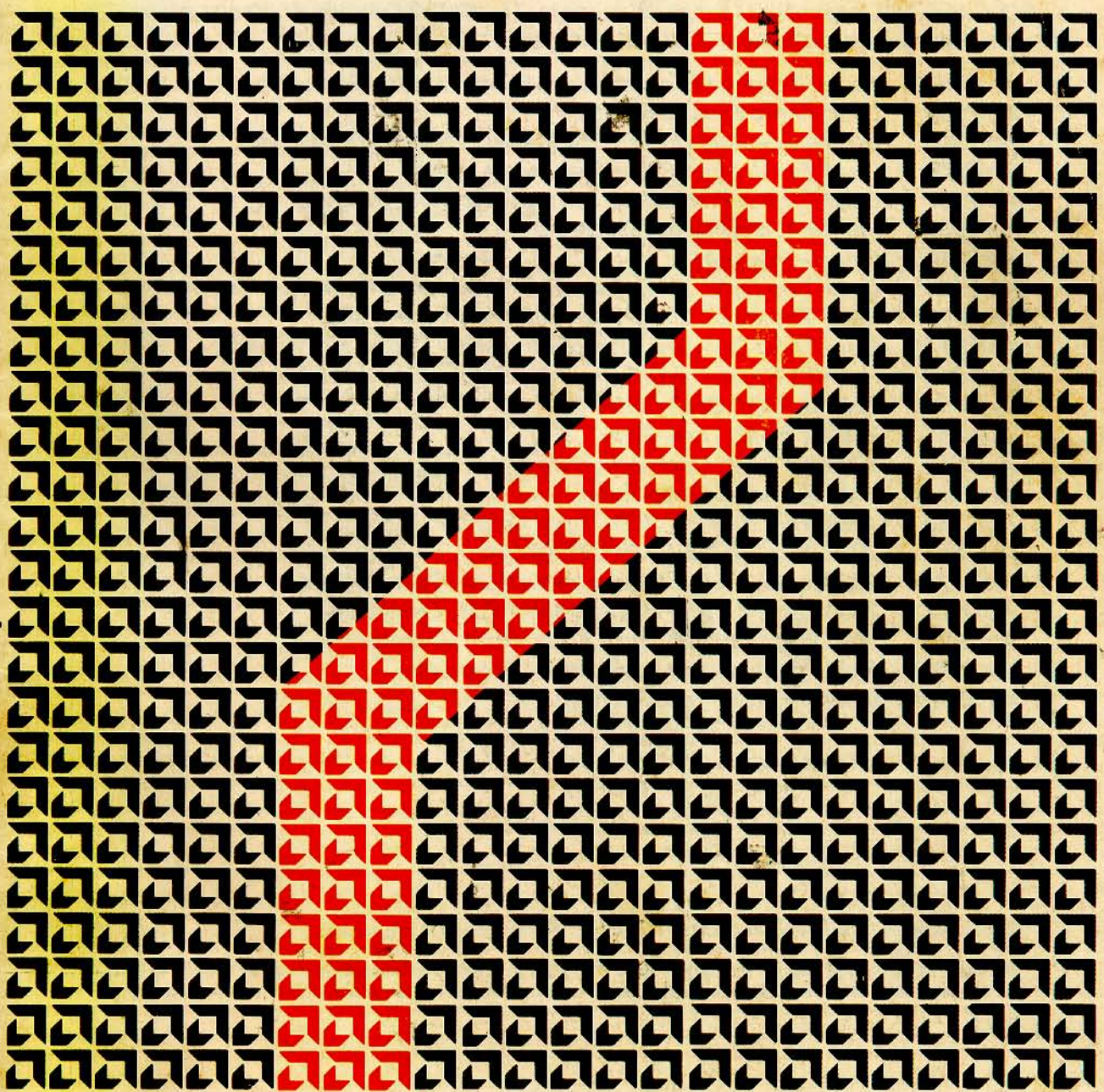
A. Baldwin

Am2900 Bipolar Microprocessor Family



The Am2900 series is a coordinated family of bipolar microprocessor circuits designed for use in high-speed digital equipment. These devices can be connected in a multiplicity of architectures to solve numerous digital computing problems. Applications include general computer or minicomputer emulation, tape or disk controllers, communications systems, voice processing machines, and a host of special purpose digital signal processors.

All circuits in Advanced Micro Devices' Am2900 family are designed to operate over the full −55°C to +125°C military operating temperature range as well as the 0°C to +70°C commercial temperature range. The Am2900 family of bipolar microprocessor circuits includes the following devices:

Am2901	*Four-Bit Bipolar Microprocessor Slice*
Am2902	*Look-Ahead Carry Generator*
Am2905	*Quad Two-Input OC Bus Transceiver, Three-State Receiver*
Am2906	*Quad Two-Input OC Bus Transceiver, Parity*
Am2907	*Quad OC Bus Transceiver, Parity, Three-State Receiver*
Am2909	*Bipolar Microprogram Sequencer*
*Am2914**	*Priority Interrupt*
*Am2915**	*Quad Two-Input Three-State Bus Transceiver, Three-State Receiver*
*Am2916**	*Quad Two-Input Three-State Bus Transceiver, Parity*
*Am2917**	*Quad Three-State Bus Transceiver, Parity, Three-State Receiver*
Am2918	*Four-Bit Register with Standard and Three-State Outputs*
Am2950	*256-Bit RAM, Open Collector*
Am2951	*256-Bit RAM, Three-State*
Am2952	*1024-Bit RAM, Open Collector*
*Am2953**	*1024-Bit RAM, Three-State*
Am2960	*1024-Word By 8-Bit ROM, Open Collector*
Am2961	*1024-Word By 8-Bit ROM, Three-State*
Am2970	*256-Word By 4-Bit Programmable ROM, Open Collector*
Am2971	*256-Word By 4-Bit Programmable ROM, Three-State*
*Am2980**	*Field Programmable Logic Array, Open Collector*
*Am2981**	*Field Programmable Logic Array, Three-State*
*Am2982**	*Bipolar First-In First-Out Memory*

* Devices currently in design. Full data will be included in the next edition of this catalog.

Advanced Micro Devices, Inc.

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Am2900 BIPOLAR MICROPROCESSOR CIRCUITS

248-8400

Cramer Prices 2 March 1976 21 May 1976 NW 1976

2901 DC — $60.00 $42.00 22.95

2902 DC $3.82

2909 DC — 25.96 16.95

2970/2971 —

2952 — (100)

BIPOLAR MICROPROCESSOR SYSTEMS

Advanced Micro Devices is committed to supplying a broad line of both bipolar and MOS microprocessor circuits. The design engineer employing these devices should recognize the performance advantages and hardware tradeoffs of each type of microprocessor as he configures the overall system. When compared with bipolar microprocessors, the MOS microprocessors are considerably slower, require fewer components to implement an operating system and have fixed macroinstruction sets. Our bipolar microprocessors are 10 to 100 times faster, require more components, consume more power and have the flexibility of being microprogrammed.

With MOS microprocessors, a minimum system may require only four to ten circuits. Most bipolar microprocessor configurations will require a minimum of thirty circuits. The advantage of the bipolar microprocessor, of course, is speed.

One of AMD's goals in configuring the Am2900 microprocessor family is to provide LSI building blocks applicable to numerous system configurations. These building blocks are well suited for computer emulation, peripheral controllers, communications and voice processors, as well as specialized dedicated digital signal processors.

Many system configurations are possible using Am2900 series IC's. As a demonstration a typical architecture of a central processing unit is shown in Figure 1. This diagram shows four distinct functions. These include the microprocessor data path (Am2901/2), the input/output bus interface transceivers (Am2905/6/7), the microprogram control (Am2909/18/60/70) and the CPU control, which includes the Am2914. The main program memory is not shown.

The Am2900 Family provides LSI building blocks for each of these typical CPU functions. The Am2901 microprocessor slice with its 16 working registers and high-speed ALU performs the various arithmetic and logic operations on the data. Some of the internal registers may be assigned as the program counter, stack pointer or other operating/control registers. The Am2905/6/7 are LSI bus transceivers that can be used to interface with the high-speed bus system. The Am2909 microprogram sequencer is designed to perform the microprogram control function. It includes an N-way branch input, instruction register, microprogram counter and 4x4 file with stack pointer for nesting microsubroutines. It functions with the microprogram memory and various registers to execute the microinstructions associated with each macroinstruction.

In addition to these devices, AMD will supply a number of PROM's, ROM's and RAM's as compatible elements for the Am2900 family. These can be used for microprogram storage, as well as macroprogram and data storage. The bipolar microprocessor circuits introduced in this catalog are the first members of the Am2900 family. Other LSI circuits are being planned. AMD is committed to making the Am2900 series the most powerful and most complete bipolar LSI family available.

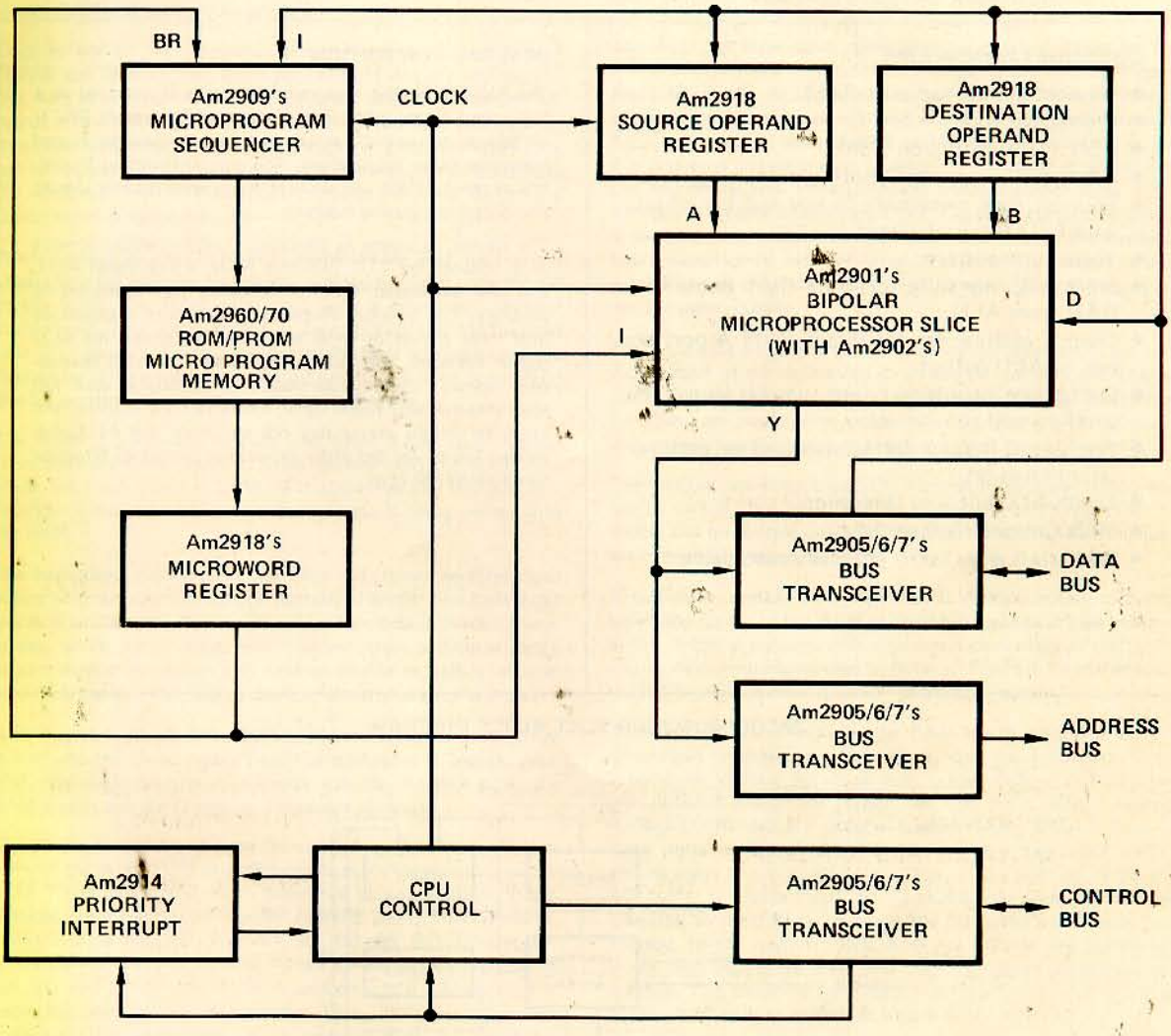


Figure 1. Typical Central Processor Unit (CPU) Using Microprogrammed High-Speed Bipolar Microprocessor Circuits.

Am2901

Four-Bit Bipolar Microprocessor Slice

PRELIMINARY DATA

Distinctive Characteristics

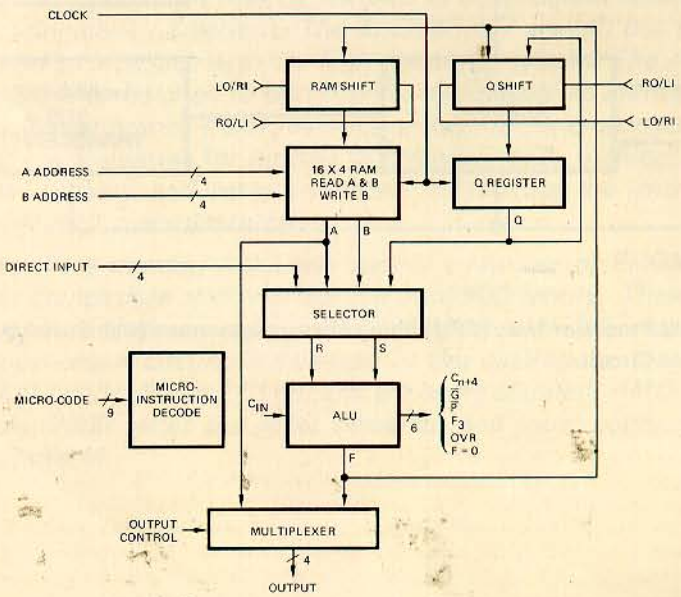
- 16-word x 4-bit two-port RAM.
- High speed ALU.
- 9-bit microinstruction word.
- Advanced low-power Schottky processing.
- Four-bit slice cascadable to any number of bits with full carry look-ahead.
- Three-state outputs.
- Shift left, no shift, or shift right entry into RAM from ALU.
- Output multiplexer for direct RAM A-port access or ALU output.
- Status flags include carry-out, sign-bit (negative), overflow and zero detect.
- Four-bit Q-register for scratch pad or accumulator extension.
- Direct ALU entry to Q-register.
- Shift Q-register left or right.
- RAM-shift and Q-shift are easily cascadable.

GENERAL DESCRIPTION

The four-bit bipolar microprocessor slice is designed as a high-speed cascadable element intended for use in CPU's, peripheral controllers, programmable microprocessors and numerous other applications. The microinstruction flexibility of the Am2901 will allow efficient emulation of almost any digital computing machine.

The device, as shown in the block diagram below, consists of a 16-word by 4-bit two-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this 40-lead LSI chip.

MICROPROCESSOR SLICE BLOCK DIAGRAM



ARCHITECTURE

A detailed block diagram of the bipolar microprogrammable microprocessor structure is shown in Figure 1. The circuit is a four-bit slice cascadable to any number of bits. Therefore, all data paths within the circuit are four bits wide. The two key elements in the Figure 1 block diagram are the 16-word by 4-bit 2-port RAM and the high-speed ALU.

Data in any of the 16 words of the Random Access Memory (RAM) can be read from the A-port of the RAM as controlled by the 4-bit A address field input. Likewise, data in any of the 16 words of the RAM as defined by the B address field input can be simultaneously read from the B-port of the RAM. The same code can be applied to the A select field and B select field in which case the identical file data will appear at both the RAM A-port and B-port outputs simultaneously.

When enabled by the RAM write enable (RAM EN), new data is always written into the file (word) defined by the B address field of the RAM. The RAM data input field is driven by a 3-input multiplexer. This configuration is used to shift the ALU output data (F) if desired. This three-input multiplexer scheme allows the data to be shifted up (right) one bit position, shifted down (left) one bit position, or not shifted in either direction.

The RAM A-port data outputs and RAM B-port data outputs drive separate 4-bit latches. These latches hold the RAM data while the clock input is LOW. This eliminates any possible race conditions that could occur while new data is being written into the RAM.

The high-speed Arithmetic Logic Unit (ALU) can perform three binary arithmetic and five logic operations on the two 4-bit input words R and S. The R input field is driven from a 2-input multiplexer, while the S input field is driven from a 3-input multiplexer. Both multiplexers also have an inhibit capability; that is, no data is passed. This is equivalent to a "zero" source operand.

Referring to Figure 1, the ALU R-input multiplexer has the RAM A-port and the direct data inputs (D) connected as inputs. Likewise, the ALU S-input multiplexer has the RAM A-port, the RAM B-port and the Q register connected as inputs.

This multiplexer scheme gives the capability of selecting various pairs of the A, B, D, Q and "0" inputs as source operands to the ALU. These five inputs, when taken two at a time, result in ten possible combinations of source operand pairs. These combinations include AB, AD, AQ, A0, BD, BQ, B0, DQ, D0 and Q0. It is apparent that AD, AQ and A0 are somewhat redundant with BD, BQ and B0 in that if the A address and B address are the same, the identical function results. Thus, there are only seven completely non-redundant source operand pairs for the ALU. The Am2901 microprocessor implements eight of these pairs. The microinstruction inputs used to select the ALU source operands are the I_0, I_1, and I_2 inputs. The definition of I_0, I_1, and I_2 for the eight source operand combinations are as shown in Figure 2. Also shown is the octal code for each selection.

The two source operands not fully described as yet are the D input and Q input. The D input is the four-bit wide direct data field input. This port is used to insert all data into the working registers inside the device. Likewise, this input can be used in the ALU to modify any of the internal data files. The Q register is a separate 4-bit file intended primarily for multiplication and division routines but it can also be used as an accumulator or holding register for some applications.

The ALU itself is a high-speed arithmetic/logic operator capable of performing three binary arithmetic and five logic functions. The I_3, I_4, and I_5 microinstruction inputs are used to select the ALU function. The definition of these inputs is shown in Figure 3. The octal code is also shown for reference. The normal technique for cascading the ALU of several devices is in a look-ahead carry mode. Carry generate, $\overline{G}$, and carry propagate, $\overline{P}$, are outputs of the device for use with a carry-look-ahead-generator such as the Am2902 ('182). A carry-out, C_{n+4}, is also generated and is available as an output for use as the carry flag in a status register. Both carry-in (C_n) and carry-out (C_{n+4}) are active HIGH.

The ALU has three other status-oriented outputs. These are F_3, F = 0, and overflow (OVR). The F_3 output is the most significant (sign) bit of the ALU and can be used to determine positive or negative results without enabling the three-state data outputs. F_3 is non-inverted with respect to the sign bit output Y_3. The F = 0 output is used for zero detect. It is an open-collector output and can be wire OR'ed between microprocessor slices. F = 0 is HIGH when all F outputs are LOW. The overflow output (OVR) is used to flag arithmetic operations that exceed the available two's complement number range. The overflow output (OVR) is HIGH when overflow exists. That is, when C_{n+3} and C_{n+4} are not the same polarity.

The ALU data output is routed to several destinations. It can be a data output of the device and it can also be stored in the RAM or the Q register. Eight possible combinations of ALU destination functions are available as defined by the I_6, I_7, and I_8 microinstruction inputs. These combinations are shown in Figure 4.

The four-bit data output field (Y) features three-state outputs and can be directly bus organized. An output control ($\overline{OE}$) is used to enable the three-state outputs. When $\overline{OE}$ is HIGH, the Y outputs are in the high-impedance state.

A two-input multiplexer is also used at the data output such that either the A-port of the RAM or the ALU outputs (F) are selected at the device Y outputs. This selection is controlled by the I_6, I_7, and I_8 microinstruction inputs. Refer to Figure 4 for the selected output for each microinstruction code combination.

As was discussed previously, the RAM inputs are driven from a three-input multiplexer. This allows the ALU outputs to be entered non-shifted, shifted up one position (X2) or shifted down one position (÷2). The shifter has two ports; one is labeled RAM_0—LO/RI and the other is labeled RAM_3—RO/LI. Both of these ports consist of a buffer-driver with a three-state output and an input to the multiplexer. Thus, in the shift up mode, the RO buffer is enabled and the RI multiplexer input is enabled. Likewise, in the shift down mode, the LO buffer and LI input are enabled. In the no-shift mode, both the LO and RO buffers are in the high-impedance state and the multiplexer inputs are not selected. This shifter is controlled from the I_6, I_7, and I_8 microinstruction inputs as defined in Figure 4.

Similarly, the Q register is driven from a 3-input multiplexer. In the no-shift mode, the multiplexer enters the ALU data into the Q register. In either the shift-up or shift-down mode, the multiplexer selects the Q register data appropriately shifted up or down. The Q shifter also has two ports; one is labeled Q_0—LO/RI and the other is Q_3—RO/LI. The operation of these two ports is similar to the RAM shifter and is also controlled from I_6, I_7, and I_8 as shown in Figure 4.

The clock input to the Am2901 controls the RAM, the Q register, and the A and B data latches. When enabled, data is clocked into the Q register on the LOW-to-HIGH transition of the clock. When the clock input is HIGH, the A and B latches are open and will pass whatever data is present at the RAM outputs. When the clock input is LOW, the latches are closed and will retain the last data entered. If the RAM-EN is enabled, new data will be written into the RAM file (word) defined by the B address field when the clock input is LOW.

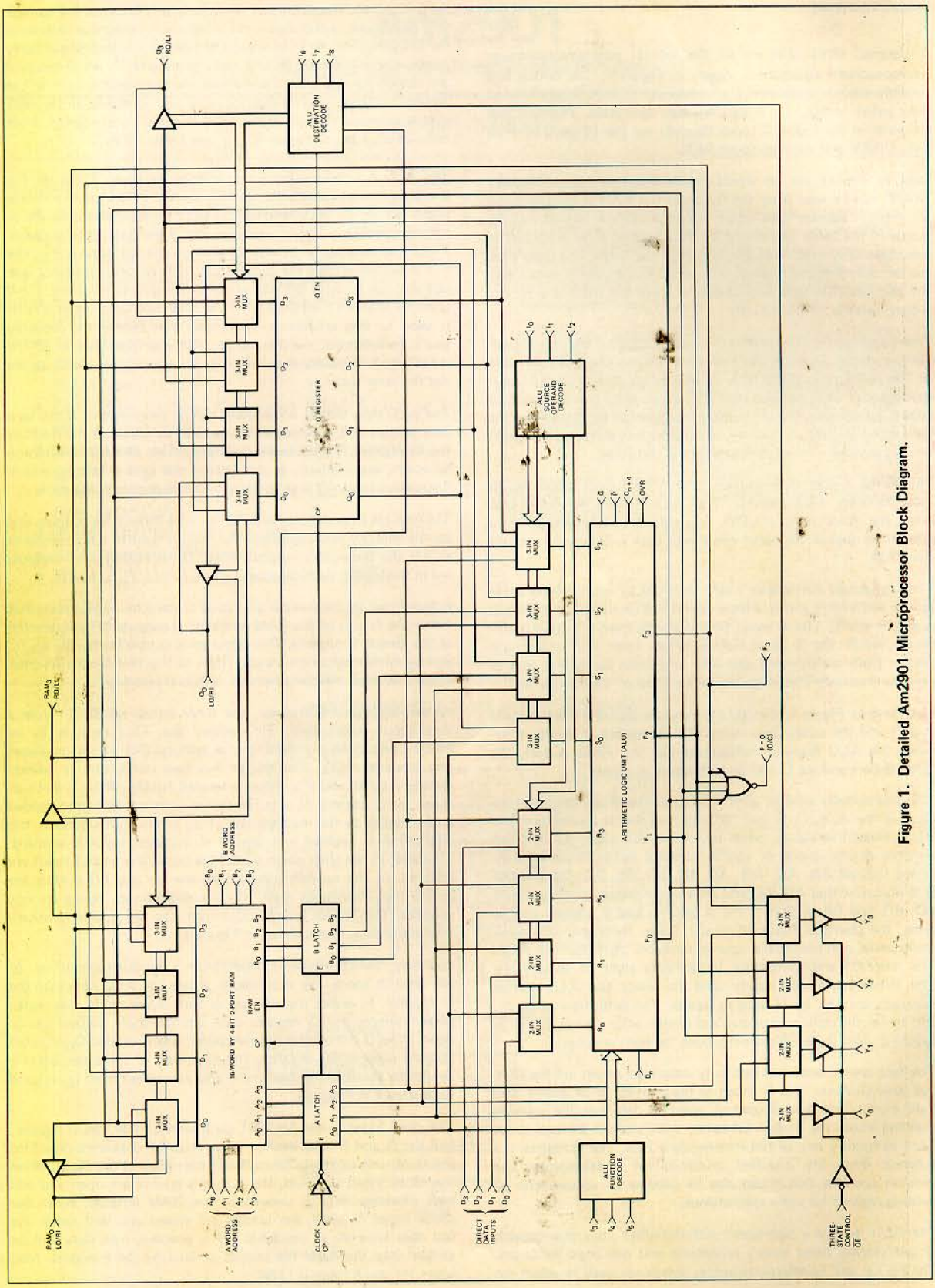


Figure 1. Detailed Am2901 Microprocessor Block Diagram.

MICRO CODE				ALU SOURCE OPERANDS	
I_2	I_1	I_0	Octal Code	R	S
L	L	L	0	A	Q
L	L	H	1	A	B
L	H	L	2	O	Q
L	H	H	3	O	B
H	L	L	4	O	A
H	L	H	5	D	A
H	H	L	6	D	Q
H	H	H	7	D	O

Figure 2. ALU Source Operand Control.

MICRO CODE				ALU Function	Symbol
I_5	I_4	I_3	Octal Code		
L	L	L	0	R Plus S	R + S
L	L	H	1	S Minus R	S − R
L	H	L	2	R Minus S	R − S
L	H	H	3	R OR S	R ∨ S
H	L	L	4	R AND S	R ∧ S
H	L	H	5	$\overline{R}$ AND S	$\overline{R}$ ∧ S
H	H	L	6	R EX-OR S	R ∀ S
H	H	H	7	R EX-NOR S	$\overline{R \forall S}$

Figure 3. ALU Function Control.

MICRO CODE				RAM FUNCTION		Q-REG. FUNCTION		Y OUTPUT	RAM SHIFTER		Q SHIFTER	
I_8	I_7	I_6	Octal Code	Shift	Load	Shift	Load		RAM_0 LO/RI	RAM_3 LI/RO	Q_0 LO/RI	Q_3 LI/RO
L	L	L	0	—	—	NONE	ALU (F_i)	F	Z	Z	Z	Z
L	L	H	1	—	—	—	—	F	Z	Z	Z	Z
L	H	L	2	NONE	ALU (F_i)	—	—	A	Z	Z	Z	Z
L	H	H	3	NONE	ALU (F_i)	—	—	F	Z	Z	Z	Z
H	L	L	4	LEFT (DOWN)	ALU (F_{i+1})	LEFT (DOWN)	Q-REG (Q_{i+1})	F	F_0	IN_3	Q_0	IN_3
H	L	H	5	LEFT (DOWN)	ALU (F_{i+1})	—	—	F	F_0	IN_3	Q_0	IN_3
H	H	L	6	RIGHT (UP)	ALU (F_{i-1})	RIGHT (UP)	Q-REG (Q_{i-1})	F	IN_0	F_3	IN_0	Q_3
H	H	H	7	RIGHT (UP)	ALU (F_{i-1})	—	—	F	IN_0	F_3	IN_0	Q_3

Z = High-Impedance

Figure 4. ALU Destination Control.

R, S / I_5 I_4 I_3 C_n		I_2 I_1 I_0	L L A, Q L	L L A, B H	L H O, Q L	L H O, B H	H L O, A L	H L D, A H	H H D, Q L	H H D, O H
			0	1	2	3	4	5	6	7
L L L L R Plus S	0	L	A+Q	A+B	Q	B	A	D+A	D+Q	D
		H	A+Q+1	A+B+1	Q+1	B+1	A+1	D+A+1	D+Q+1	D+1
L L H L S Minus R	1	L	Q−A−1	B−A−1	Q−1	B−1	A−1	A−D−1	Q−D−1	−D−1
		H	Q−A	B−A	Q	B	A	A−D	Q−D	−D
L H L L R Minus S	2	L	A−Q−1	A−B−1	−Q−1	−B−1	−A−1	D−A−1	D−Q−1	D−1
		H	A−Q	A−B	−Q	−B	−A	D−A	D−Q	D
L H H L R OR S	3	L	A ∨ Q	A ∨ B	Q	B	A	D ∨ A	D ∨ Q	D
		H								
H L L L R AND S	4	L	A ∧ Q	A ∧ B	0	0	0	D ∧ A	D ∧ Q	0
		H								
H L H L $\overline{R}$ AND S	5	L	$\overline{A}$ ∧ Q	$\overline{A}$ ∧ B	Q	B	A	$\overline{D}$ ∧ A	$\overline{D}$ ∧ Q	0
		H								
H H L L R EX-OR S	6	L	A ∀ Q	A ∀ B	Q	B	A	D ∀ A	D ∀ Q	D
		H								
H H H L R EX-NOR S	7	L	$\overline{A \forall Q}$	$\overline{A \forall B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \forall A}$	$\overline{D \forall Q}$	$\overline{D}$
		H								

+ = Plus; − = Minus; ∨ = OR; ∧ = AND; ∀ = EX-OR

Figure 5. Source Operand and ALU Function Matrix.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +6.3V
DC Voltage Applied to Outputs for HIGH Output State	+0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

Am2901XC T_A = 0°C to +70°C V_{CC} = 5.0V ±5% (COM'L) MIN. = 4.75V MAX. = 5.25V
Am2901XM T_A = −55°C to +125°C V_{CC} = 5.0V ±10% (MIL) MIN. = 4.5V MAX. = 5.5V

(Preliminary Data)

Parameters	Description	Test Conditions (Note 1)		MIL Min.	MIL Typ. (Note 2)	MIL Max.	COM'L Min.	COM'L Typ. (Note 2)	COM'L Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −1.6mA Y_0, Y_1, Y_2, Y_3	2.4			2.4			Volts
			I_{OH} = −1.0mA, C_{n+4}	2.5			2.7			
			I_{OH} = −800μA, OVR, $\overline{P}$	2.5			2.7			
			I_{OH} = −600μA, F_3	2.5			2.7			
			I_{OH} = −600μA All RO/LI, LO/RI	2.4			2.4			
			I_{OH} = −1.6mA, $\overline{G}$	2.5			2.7			
I_{OH}	Output HIGH Current for F = 0 Output	V_{CC} = MIN., V_{OH} = 5.5V V_{IN} = V_{IH} or V_{IL}				250			250	μA
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 16mA $Y_0, Y_1, Y_2, Y_3, \overline{G}$			0.5			0.5	Volts
			I_{OL} = 10mA, C_{n+4}, F=0			0.5			0.5	
			I_{OL} = 8.0mA, OVR, $\overline{P}$			0.5			0.5	
			I_{OL} = 6.0mA, F_3 All RO/LI, LO/RI			0.5			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.7			0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA				−1.5			−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX. V_{IN} = 0.5V	Clock, $\overline{OE}$			−0.36			−0.36	mA
			A_0, A_1, A_2, A_3			−0.36			−0.36	
			B_0, B_1, B_2, B_3			−0.36			−0.36	
			D_0, D_1, D_2, D_3			−0.36			−0.36	
			I_0, I_1, I_2, I_6, I_7			−0.36			−0.36	
			I_3, I_4, I_5, I_8			−0.72			−0.72	
			All LO/RI, RO/LI			−0.72			−0.72	
			C_n			−5.4			−5.4	
I_{IH}	Input HIGH Current	V_{CC} = MAX.	Clock, $\overline{OE}$			20			20	μA
			A_0, A_1, A_2, A_3			20			20	
			B_0, B_1, B_2, B_3			20			20	
			D_0, D_1, D_2, D_3			20			20	
			I_0, I_1, I_2, I_6, I_7			20			20	
			I_3, I_4, I_5, I_8			40			40	
			All LO/RI, RO/LI			100			100	
			C_n			300			300	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0			1.0	mA
I_O	Off State (High Impedance) Output Current	V_{CC} = MAX.	Y_0, Y_1, Y_2, Y_3 V_O = 2.4V			50			50	μA
			Y_0, Y_1, Y_2, Y_3 V_O = 0.5V			−50			−50	
			All LO/RI, RO/LI V_O = 2.4V (Note 4)			100			100	
			All LO/RI, RO/LI V_O = 0.5V (Note 4)			−720			−720	
I_{SC}	Output Short Circuit Current (Note 3)		$Y_0, Y_1, Y_2, Y_3, \overline{G}$	−6.0		−40	−5.0		−42	mA
			C_{n+4}	−6.0		−40	−5.0		−42	
			OVR, $\overline{P}$	−6.0		−40	−5.0		−42	
			F_3	−6.0		−40	−5.0		−42	
			All RO/LI, LO/RI	−6.0		−40	−5.0		−42	
I_{CC}	Power Supply Current	V_{CC} = MAX.			185			185		mA

Notes:
1. For conditions shown as MIN or MAX, use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. Measured with RO and LO buffers in the high-impedance state.

Switching Characteristics (T_A = +25°C, V_{CC} = 5V, R_L = 2kΩ, C_L = 15pF, $t_r = t_f \leq 2.5$ ns)

(Preliminary Data)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units	Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	A or B Address to any Y_i ALU Logic Mode			60		ns	t_{PLH}	I_{012} to Y_i Sum Mode			44		ns
t_{PHL}				60		ns	t_{PHL}				44		ns
t_{PLH}	A or B Address to any Y_i ALU Sum Mode			65		ns	t_{PLH}	I_{012} to Y_i Diff Mode			44		ns
t_{PHL}				65		ns	t_{PHL}				44		ns
t_{PLH}	A or B Address to any Y_i ALU Diff Mode			65		ns	t_{PLH}	I_{345} to Y_i			37		ns
t_{PHL}				65		ns	t_{PHL}				37		ns
t_{PLH}	A Address to any Y_i via RAM A-Port			38		ns	t_{PLH}	I_{345} to C_{n+4}			32		ns
t_{PHL}				38		ns	t_{PHL}				32		ns
t_{PLH}	A or B Address to $\overline{G}$			53		ns	t_{PLH}	I_{678} to LO or RO			25		ns
t_{PHL}				53		ns	t_{PHL}				25		ns
t_{PLH}	A or B Address to $\overline{P}$			53		ns	t_{PLH}	I_{678} to Y_i			30		ns
t_{PHL}				53		ns	t_{PHL}				30		ns
t_{PLH}	A or B Address to C_{n+4}			60		ns	t_{PLH}	C_n to C_{n+4}			20		ns
t_{PHL}				60		ns	t_{PHL}				20		ns
t_{PLH}	A or B Address to OVR			63		ns	t_{PLH}	C_n to OVR			25		ns
t_{PHL}				63		ns	t_{PHL}				25		ns
t_{PLH}	A or B Address to F = 0			64		ns	t_{PLH}	C_n to F_3			20		ns
t_{PHL}				64		ns	t_{PHL}				20		ns
t_{PLH}	A or B Address to F_3			53		ns	t_{PLH}	C_n to RO or LO			37		ns
t_{PHL}				53		ns	t_{PHL}				37		ns
t_{PLH}	A or B Address to RAM RO or LO			65		ns	t_{PLH}	C_n to F = 0			35		ns
t_{PHL}				65		ns	t_{PHL}				35		ns
t_{PLH}	D_i to any Y_i ALU Logic Mode			32		ns	t_{PLH}	C_n to Y_i			35		ns
t_{PHL}				32		ns	t_{PHL}				35		ns
t_{PLH}	D_i to any Y_j ALU Sum Mode	$i \leq j$		37		ns	t_s	D_i to Clock			27		ns
t_{PHL}				37		ns	t_h				−25		ns
t_{PLH}	D_i to any Y_j ALU Diff Mode			37		ns	t_s	C_n to Clock			25		ns
t_{PHL}				37		ns	t_h				−23		ns
t_{PLH}	D_i to $\overline{G}$			25		ns	t_s	RAM_0-RI or RAM_3-LI to Clock			1.0		ns
t_{PHL}				25		ns	t_h				1.0		ns
t_{PLH}	D_i to $\overline{P}$			25		ns	t_s	Q_0-RI or Q_3-LI to Clock			1.0		ns
t_{PHL}				25		ns	t_h				1.0		ns
t_{PLH}	D_i to C_{n+4}			32		ns	t_s	I_{012} to Clock			34		ns
t_{PHL}				32		ns	t_h				−32		ns
t_{PLH}	D_i to OVR			35		ns	t_s	I_{345} to Clock			27		ns
t_{PHL}				35		ns	t_h				−25		ns
t_{PLH}	D_i to F = 0			36		ns	t_s	I_{678} to $\overline{\text{Clock}}$			13		ns
t_{PHL}				36		ns	t_h	I_{678} to Clock					ns
t_{PLH}	D_i to F_3			25		ns	t_s	A Address to $\overline{\text{Clock}}$			20		ns
t_{PHL}				25		ns	t_h				−18		ns
t_{PLH}	D_i to RO or LO			37		ns	t_s	B Address to $\overline{\text{Clock}}$			20		ns
t_{PHL}				37		ns	t_h	B Address to Clock					ns
t_{PLH}	Clock to Y_i via Q Register			67		ns	t_{pw}	Clock LOW			10		ns
t_{PHL}				67		ns		Clock HIGH			10		ns
t_{PLH}	Clock to C_{n+4} via Q Register			62		ns	t_{ZH}	Output Control ($\overline{OE}$) to Y_i			14		ns
t_{PHL}				62		ns	t_{ZL}				14		ns
t_{PLH}	I_{012} to Y_i Logic Mode			39		ns	t_{HZ}				14		ns
t_{PHL}				39		ns	t_{LZ}				14		ns

Notes: 1. CLOCK = LOW-to-HIGH transition.
2. $\overline{\text{CLOCK}}$ = HIGH-to-LOW transition.
3. I_{678} and B address should not change while the clock is LOW.

SOURCE OPERANDS AND ALU FUNCTIONS

As discussed earlier, there are eight source operand pairs available to the ALU as selected by the I_0, I_1, and I_2 instruction inputs. The ALU can perform eight functions; five logic and three arithmetic. The I_3, I_4, and I_5 instruction inputs control this function selection. The carry input, C_n, also affects the ALU results when in the arithmetic mode. The C_n input is inhibited in the logic mode. When I_0 through I_5 and C_n are viewed together, the matrix of Figure 5 results. This matrix fully defines the ALU/source operand function for each state.

The ALU functions can also be examined on a "task" basis, i.e., add, subtract, AND, OR, etc. In the arithmetic mode, the carry will affect the function performed while in the logic mode, the carry will have no bearing on the ALU output. Figure 6 defines the various logic operations that the Am2901 can perform and Figure 7 shows the arithmetic functions of the device. Both carry-in LOW (C_n = 0) and carry-in HIGH (C_n = 1) are defined in these operations.

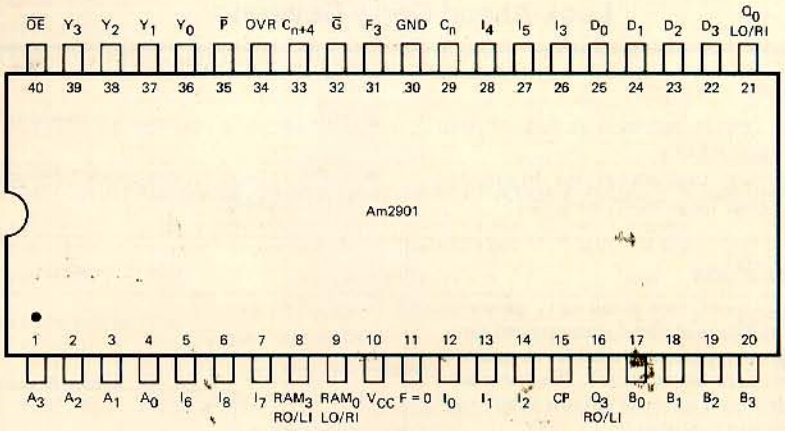
$I_5I_4I_3I_2I_1I_0$	Octal I_{543}, I_{210}	Group	Function
1 0 0 0 0 0	40	AND	A∧Q
0 0 1	41		A∧B
1 0 1	45		D∧A
1 1 0	46		D∧Q
0 1 1 0 0 0	30	OR	A∨Q
0 0 1	31		A∨B
1 0 1	35		D∨A
1 1 0	36		D∨Q
1 1 0 0 0 0	60	EX-OR	A∀Q
0 0 1	61		A∀B
1 0 1	65		D∀A
1 1 0	66		D∀Q
1 1 1 0 0 0	70	EX-NOR	$\overline{A \forall Q}$
0 0 1	71		$\overline{A \forall B}$
1 0 1	75		$\overline{D \forall A}$
1 1 0	76		$\overline{D \forall Q}$
1 1 1 0 1 0	72	INVERT	$\overline{Q}$
0 1 1	73		$\overline{B}$
1 0 0	74		$\overline{A}$
1 1 1	77		$\overline{D}$
1 1 0 0 1 0	62	PASS	Q
0 1 1	63		B
1 0 0	64		A
1 1 1	67		D
0 1 1 0 1 0	32	PASS	Q
0 1 1	33		B
1 0 0	34		A
1 1 1	37		D
1 0 0 0 1 0	42	"ZERO"	0
0 1 1	43		0
1 0 0	44		0
1 1 1	47		0
1 0 1 0 0 0	50	MASK	$\overline{A}$∧Q
0 0 1	51		$\overline{A}$∧B
1 0 1	55		$\overline{D}$∧A
1 1 0	56		$\overline{D}$∧Q

Figure 6. ALU Logic Mode Functions.

$I_5I_4I_3I_2I_1I_0$	Octal I_{543}, I_{210}	C_n = 0 Group	C_n = 0 Function	C_n = 1 Group	C_n = 1 Function
0 0 0 0 0 0	0 0	ADD	A+Q	ADD plus one	A+Q+1
0 0 1	0 1		A+B		A+B+1
1 0 1	0 5		D+A		D+A+1
1 1 0	0 6		D+Q		D+Q+1
0 0 0 0 1 0	0 2	PASS	Q	Increment	Q+1
0 1 1	0 3		B		B+1
1 0 0	0 4		A		A+1
1 1 1	0 7		D		D+1
0 0 1 0 1 0	1 2	Decrement	Q−1	PASS	Q
0 1 1	1 3		B−1		B
1 0 0	1 4		A−1		A
0 1 0 1 1 1	2 7		D−1		D
0 1 0 0 1 0	2 2	1's Comp.	−Q−1	2's Comp.	−Q
0 1 1	2 3		−B−1		−B
1 0 0	2 4		−A−1		−A
0 0 1 1 1 1	1 7		−D−1		−D
0 0 1 0 0 0	1 0	Subtract (1's Comp)	Q−A−1	Subtract (2's Comp)	Q−A
0 0 1	1 1		B−A−1		B−A
1 0 1	1 5		A−D−1		A−D
1 1 0	1 6		Q−D−1		Q−D
0 1 0 0 0 0	2 0		A−Q−1		A−Q
0 0 1	2 1		A−B−1		A−B
1 0 1	2 5		D−A−1		D−A
1 1 0	2 6		D−Q−1		D−Q

Figure 7. ALU Arithmetic Mode Functions.

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

Final Data. The preliminary data sheet printed 3-78 had pins 5 and 6 interchanged and pins 12 and 14 interchanged when compared with the above connection diagram.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	0°C to +70°C	AM2901DC
Dice	0°C to +70°C	AM2901XC
Hermetic DIP	−55°C to +125°C	AM2901DM
Dice	−55°C to +125°C	AM2901XM

FURTHER INFORMATION

If additional preliminary technical information is required, contact the nearest AMD Sales Office or call the factory in Sunnyvale, California and ask for

JOHN SPRINGER
Marketing Manager
Bipolar Microprocessor Circuits
(408) 732-2400 or toll free from outside California (800) 538-7904 or 538-7989.

Am2902

Look-Ahead Carry Generator

Distinctive Characteristics

- Provides look-ahead carries across a group of four Am2901 microprocessor ALU's
- Capability of multi-level look-ahead for high-speed arithmetic operation over large word lengths
- Typical carry propagation delay of 6 ns
- 100% reliability assurance testing in compliance with MIL-STD-882.

FUNCTIONAL DESCRIPTION

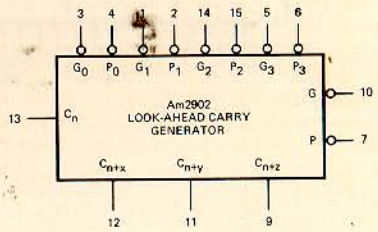
The Am2902 is a high-speed, look-ahead carry generator which accepts up to four pairs of carry propagate and carry generate signals and a carry input and provides anticipated carries across four groups of binary ALU's. The device also has carry propagate and carry generate outputs which may be used for further levels of look-ahead.

The Am2902 is generally used with the 2901 bipolar microprocessor unit to provide look-ahead over word lengths of more than four bits. The look-ahead carry generator can be used with binary ALU's in an active LOW or active HIGH input operand mode by reinterpreting the carry functions. The connections to and from the ALU to the look-ahead carry generator are identical in both cases.

The logic equations provided at the outputs are:

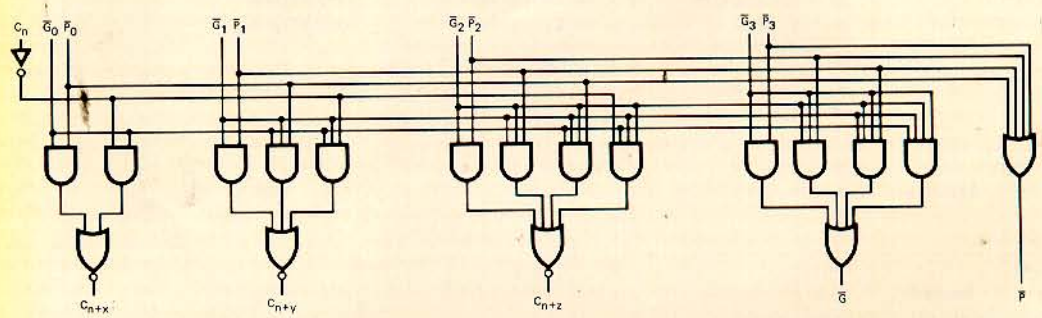
$$C_{n+x} = G_0 + P_0C_n$$
$$C_{n+y} = G_1 + P_1G_0 + P_1P_0C_n$$
$$C_{n+z} = G_2 + P_2G_1 + P_2P_1G_0 + P_2P_1P_0C_n$$
$$G = G_3 + P_3G_2 + P_3P_2G_1 + P_3P_2P_1G_0$$
$$P = P_3P_2P_1P_0$$

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

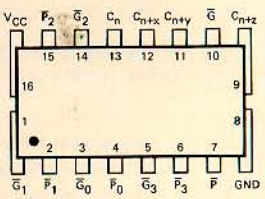
LOGIC DIAGRAM



ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2902PC
Hermetic DIP	0°C to +70°C	AM2902DC
Dice	0°C to +70°C	AM2902XC
Hermetic DIP	−55°C to +125°C	AM2902DM
Hermetic Flat Pack	−55°C to +125°C	AM2902FM
Dice	−55°C to +125°C	AM2902XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7.0V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2902XC	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am2902XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10% (MIL)	MIN. = 4.50V	MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = −0.8mA V_{IN} = V_{IH} or V_{IL}		2.4	3.0		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 16mA V_{IN} = V_{IH} or V_{IL}			0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −12mA				−1.5	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V	C_n			−3.2	mA
			$\overline{P}_3$			−4.8	
			$\overline{P}_2$			−6.4	
			$\overline{P}_0, \overline{P}_1, \overline{G}_3$			−8.0	
			$\overline{G}_0, \overline{G}_2$			−14.4	
			$\overline{G}_1$			−16	
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V	C_n			80	µA
			$\overline{P}_3$			120	
			$\overline{P}_2$			160	
			$\overline{P}_0, \overline{P}_1, \overline{G}_3$			200	
			$\overline{G}_0, \overline{G}_2$			360	
			$\overline{G}_1$			400	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V				1.0	mA
I_{SC}	Output Short Circuit (Note 4)	V_{CC} = MAX., V_{OUT} = 0.0V		−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. All Outputs LOW	MIL		45	65	mA
			COM'L		45	72	
		V_{CC} = MAX. All Ouputs HIGH	MIL		27		mA
			COM'L		27		

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current X Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS V_{CC} = 5.0V, T_A = 25°C, C_L = 15pF, R_L = 400Ω

Parameter	From (Input)	To (Output)	Test Figure	Test Conditions	Min	Typ	Max	Units
t_{PLH}	C_n	C_{n+j}	2	$\overline{P}_0 = \overline{P}_i = \overline{P}_2 = 0$ V $\overline{G}_0 = \overline{G}_i = \overline{G}_2 = 4.5$ V		11	14	ns
t_{PHL}						11	14	
t_{PLH}	$\overline{P}_i$	C_{n+j}	3	$\overline{P}_i = 0$ V (j ≥ i) $C_n = \overline{G}_0 = \overline{G}_i = \overline{G}_2 = 4.5$ V		6.0	8.0	ns
t_{PHL}						6.0	8.0	
t_{PLH}	$\overline{G}_i$	C_{n+j}	3	$\overline{G}_i = 0$ V (j ≥ i) $C_n = \overline{P}_0 = \overline{P}_i = \overline{P}_2 = 4.5$ V		6.0	8.0	ns
t_{PHL}						6.0	8.0	
t_{PLH}	$\overline{P}_i$	$\overline{G}$ or $\overline{P}$	2	$\overline{P}_i = 0$ V (j ≥ i) $C_n = \overline{G}_0 = \overline{G}_i = \overline{G}_2 = 4.5$ V		11	14	ns
t_{PHL}						11	14	
t_{PLH}	$\overline{G}_i$	$\overline{G}$ or $\overline{P}$	2	$\overline{G}_i = 0$ V (j ≥ i) $C_n = \overline{P}_0 = \overline{P}_i = \overline{P}_2 = 4.5$ V		12	14	ns
t_{PHL}						12	14	

DEFINITION OF FUNCTIONAL TERMS

C_n Carry-in. The carry-in input to the look-ahead generator. Also the carry-in input to the nth Am2901 microprocessor ALU input.

C_{n+j} Carry-out. (j = x, y, z). The carry-out output to be used at the carry-in inputs of the n+1, n+2 and n+3 microprocessor ALU slices.

G_i, P_i Generate and propagate inputs respectively (i = 0, 1, 2, 3). The carry generate and carry propagate inputs from the n, n+1, n+2 and n+3 microprocessor ALU slices.

G, P Generate and propagate outputs respectively. The carry generate and carry propagate outputs that can be used with the next higher level of carry look-ahead if used.

TRUTH TABLE

Inputs									Outputs				
C_n	$\overline{G}_0$	$\overline{P}_0$	$\overline{G}_1$	$\overline{P}_1$	$\overline{G}_2$	$\overline{P}_2$	$\overline{G}_3$	$\overline{P}_3$	C_{n+x}	C_{n+y}	C_{n+z}	$\overline{G}$	$\overline{P}$
X	H	H							L				
L	H	X							L				
X	L	X							H				
H	X	L							H				
X	X	X	H	H						L			
X	H	H	H	X						L			
L	H	X	H	X						L			
X	X	X	L	X						H			
X	L	X	X	L						H			
H	X	L	X	L						H			
X	X	X	X	H	H	H					L		
X	H	H	H	X	H	X					L		
L	H	X	H	X	H	X					L		
X	X	X	L	X	X	L					H		
X	X	X	X	L	X	L					H		
H	X	L	X	L	X	L					H		
	X		X	X	X	X	H	H				H	
	X		X	X	H	H	H	X				H	
	X		H	H	H	X	H	X				H	
	H		H	X	X	X	H	X				H	
	X		X	X	X	X	L	X				L	
	X		X	X	L	X	X	L				L	
	X		X	X	X	L	X	L				L	
	L		X	L	L	L	X	L				L	
		H	X		X		X						H
		X	H		X		X						H
		X	X		H		X						H
		X	X		X		H						H
		L	X		L		L						L

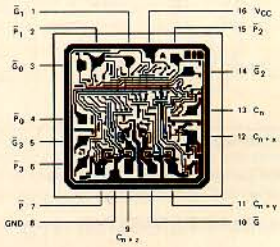
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{G_1}$	1	8.0	–	–
$\overline{P_1}$	2	4.0	–	–
$\overline{G_0}$	3	7.2	–	–
$\overline{P_0}$	4	4.0	–	–
$\overline{G_3}$	5	4.0	–	–
$\overline{P_3}$	6	2.4	–	–
$\overline{P}$	7	–	16	8
GND	8	–	–	–
C_{n+z}	9	–	16	8
$\overline{G}$	10	–	16	8
C_{n+y}	11	–	16	8
C_{n+x}	12	–	16	8
C_n	13	1.6	–	–
$\overline{G_2}$	14	7.2	–	–
$\overline{P_2}$	15	3.2	–	–
V_{CC}	16	–	–	–

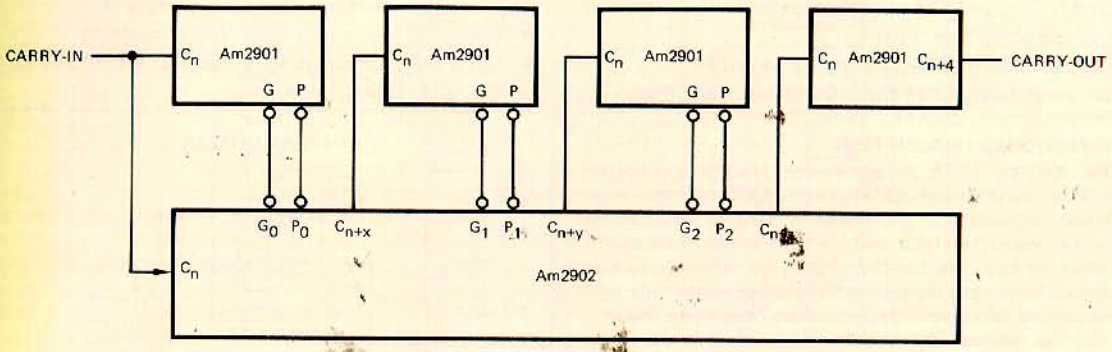
A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

Metallization and Pad Layout

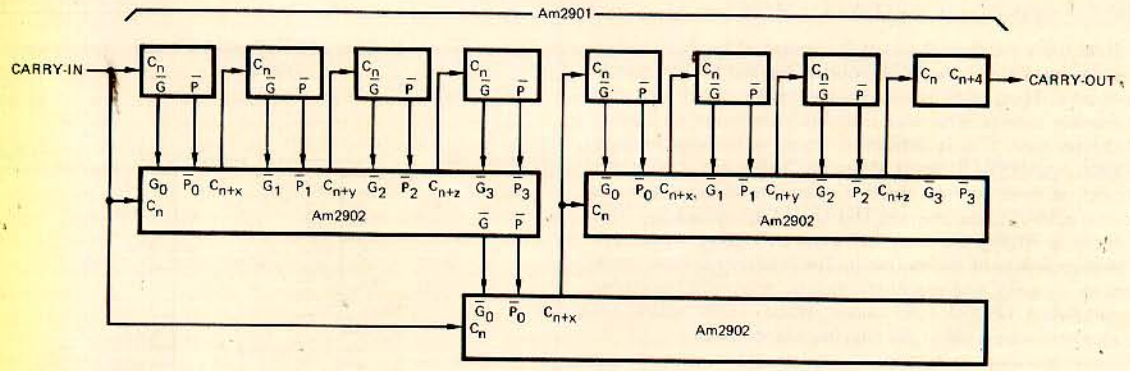


DIE SIZE 0.068" X 0.068"

APPLICATIONS



16-BIT CARRY LOOK-AHEAD CONNECTION.



32-BIT ALU, THREE LEVEL CARRY LOOK-AHEAD.

Am2905

Quad Two-Input OC Bus Transceiver With Three-State Receiver

PRELIMINARY DATA

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver
- Two-port input to D-type register on driver
- Bus driver output can sink 100 mA at 0.8V max.
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced low-power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2905 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches that feature three-state outputs.

This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

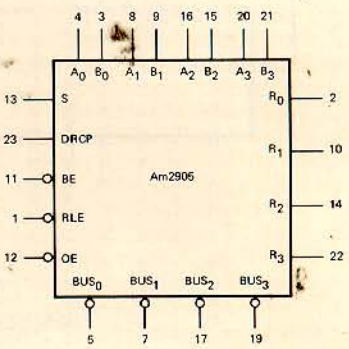
The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B inputs is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

ORDERING INFORMATION

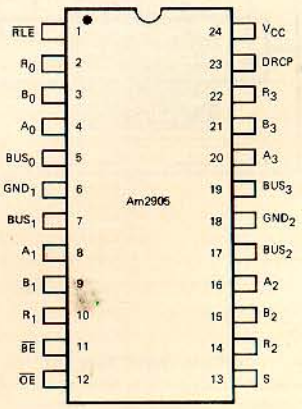
Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2905PC
Hermetic DIP	0°C to +70°C	AM2905DC
Dice	0°C to +70°C	AM2905XC
Hermetic DIP	−55°C to +125°C	AM2905DM
Hermetic Flat Pak	−55°C to +125°C	AM2905FM
Dice	−55°C to +125°C	AM2905XM

LOGIC SYMBOL



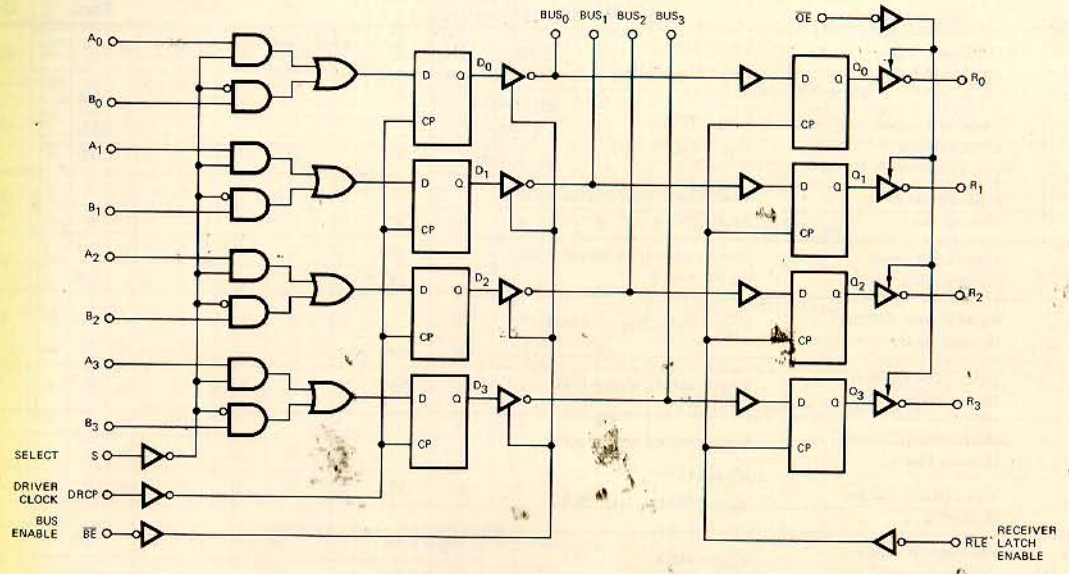
V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	200mA
DC Input Current	−30mA to +5.0mA

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Am2905XC	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5%(COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am2905XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%(MIL)	MIN. = 4.50V	MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	MIL	I_{OL} = 40mA			0.5	Volts
				I_{OL} = 70mA			0.8	
				I_{OL} = 100mA			1.0	
			COM'L	I_{OL} = 40mA			0.5	
				I_{OL} = 70mA			0.7	
				I_{OL} =100mA			0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	µA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	µA
V_{TH}	Receiver Input HIGH Threshold	Bus enable = 2.4V			2.3	2.0		Volts
V_{TL}	Receiver Input LOW Threshold	Bus enable = 2.4V				2.0	1.7	Volts

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2905XC	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$ (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am2905XM	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$ (MIL)	MIN. = 4.50V	MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)		Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL $I_{OH} = -1mA$	2.4	3.4		Volts
			COM'L $I_{OH} = -2.6mA$	2.4	3.4		
V_{OL}	Receiver Output LOW Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	$I_{OL} = 4mA$			0.4	Volts
			$I_{OL} = 8mA$			0.45	
			$I_{OL} = 12mA$			0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs		2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs	MIL			0.7	Volts
			COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18mA$				−1.5	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4V$				−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7V$				20	µA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 5.5V$				100	µA
I_O	Receiver Off-State Output Current	V_{CC} = MAX.	$V_O = 2.4V$			20	µA
			$V_O = 0.4V$			−20	
I_{SC}	Receiver Output Short Circuit Current	V_{CC} = MAX. (Note 3)	MIL	−6.0		−40	mA
			COM'L	−5.0		−42	
I_{CC}	Power Supply Current	V_{CC} = MAX., All inputs = GND			69		mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS ($T_A = +25°C$) — PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L(BUS) = 50pF, R_L(BUS) = 50Ω		21		ns
t_{PLH}				21		
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13		ns
t_{PLH}				13		
t_s	Data Inputs (A or B)	C_L = 15pF, R_L = 2kΩ	20			ns
t_h			5.0			
t_s	Select Input (S)		30			ns
t_h			5.0			
t_{PW}	Driver Clock (DRCP) Pulse Width (HIGH)		20			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			17		ns
t_{PHL}				17		
t_{PLH}	Latch Enable to Receiver Output			15		ns
t_{PHL}				15		
t_s	Bus to Latch Enable ($\overline{RLE}$)		15			ns
t_h			0			
t_{ZH}	Output Control to Receiver Output	C_L = 15pF, R_L = 2kΩ		10		ns
t_{ZL}				14		
t_{HZ}	Output Control to Receiver Output			10		ns
t_{LZ}				9		

FUNCTION TABLE

INPUTS							INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	B_i	R_i	
X	X	X	X	H	X	X	X	X	H	X	Driver output disable
X	X	X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	L	X	H	H	L	
X	X	X	X	X	H	X	X	NC	X	X	Latch received data
L	L	X	↑	X	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	X	H	X	X	X	
H	X	L	↑	X	X	X	L	X	X	X	
H	X	H	↑	X	X	X	H	X	X	X	
X	X	X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	X	NC	X	X	X	
X	X	X	X	L	X	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	X	H	X	L	X	

H = HIGH
L = LOW
Z = HIGH Impedance
NC = No change
X = Don't care
↑ = LOW-to-HIGH transition
i = 0, 1, 2, 3

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexer of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is LOW, the four drivers are in the high impedance state.

BUS_0, BUS_1 BUS_2, BUS_3 The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When RLE is LOW, data on the BUS inputs is passed through the receiver latches. When RLE is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

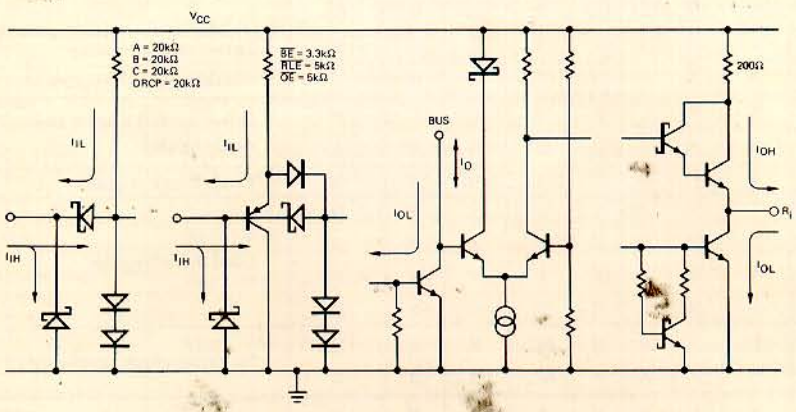
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three state receiver outputs are in the high-impedance state.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{RLE}$	1	1	–	–
R_0	2	–	50/130	33
B_0	3	1	–	–
A_0	4	1	–	–
BUS_0	5	–	OC	BUS
GND_1	6	–	–	–
BUS_1	7	–	OC	BUS
A_1	8	1	–	–
B_1	9	1	–	–
R_1	10	–	50/130	33
$\overline{BE}$	11	1	–	–
$\overline{OE}$	12	1	–	–
S	13	1	–	–
R_2	14	–	50/130	33
B_2	15	1	–	–
A_2	16	1	–	–
BUS_2	17	–	OC	BUS
GND_2	18	–	–	–
BUS_3	19	–	OC	BUS
A_3	20	1	–	–
B_3	21	1	–	–
R_3	22	–	50/130	33
DRCP	23	1	–	–
V_{CC}	24	–	–	–

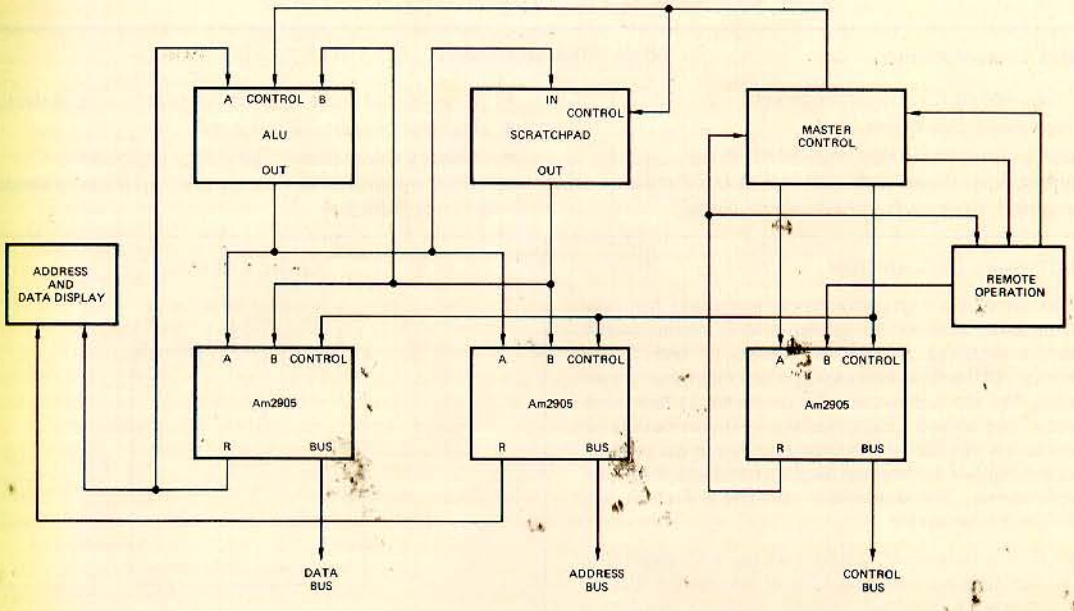
A Low Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

APPLICATIONS



The Am2905 is a universal Bus Transceiver useful for many system data, address, control and timing input/output interfaces.

Am2906

Quad Two-Input OC Bus Transceiver With Parity

Distinctive Characteristics PRELIMINARY DATA

- Quad high-speed LSI bus-transceiver.
- Open-collector bus driver.
- Two-port input to D-type register on driver.
- Bus driver output can sink 100 mA at 0.8V max.
- Internal odd 4-bit parity checker/generator.
- Receiver has output latch for pipeline operation.
- Receiver outputs sink 12 mA.
- Advanced low-power Schottky processing.
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am2906 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops with a built-in two-input multiplexer on each. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches. The device also contains a four-bit odd parity checker/generator.

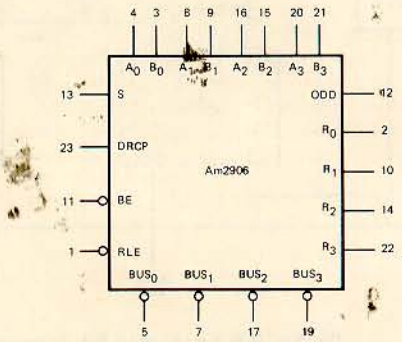
This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock and a two-input multiplexer at the input of each flip-flop. A common select input (S) controls the four multiplexers. When S is LOW, the A_i data is stored in the register and when S is HIGH, the B_i data is stored. The buffered common clock (DRCP) enters the data into this driver register on the LOW-to-HIGH transition.

Data from the A or B input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input.

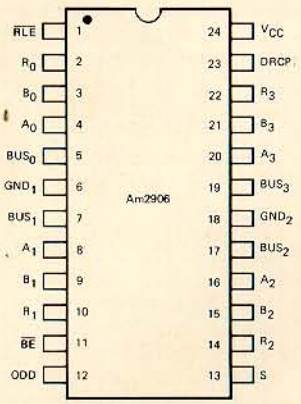
The Am2906 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A or B field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

LOGIC SYMBOL



V_{CC} = Pin 24
GND_1 = Pin 6
GND_2 = Pin 18

CONNECTION DIAGRAM
Top View

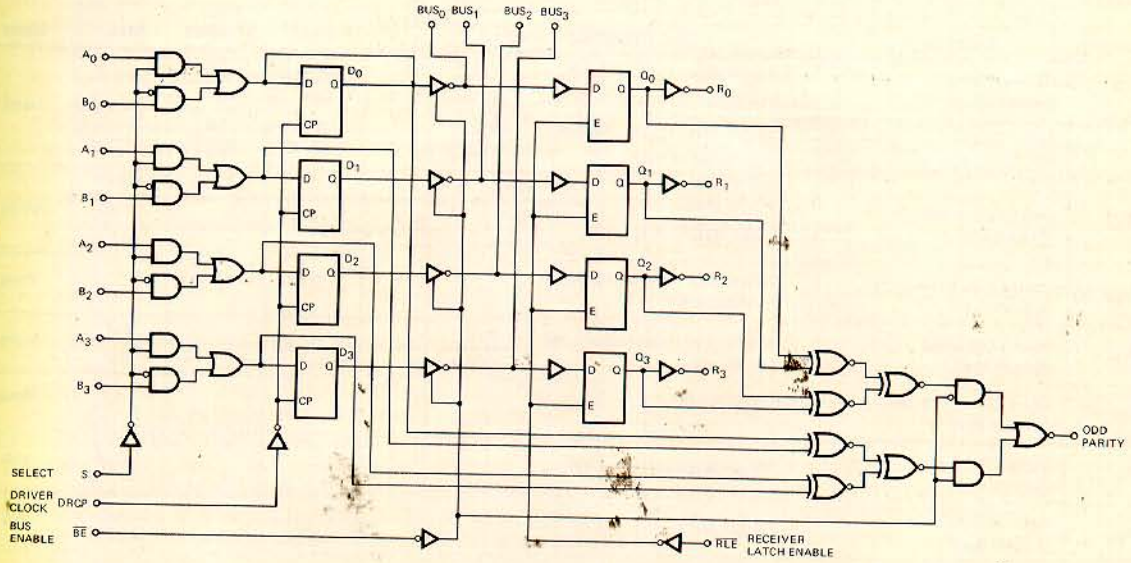


Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2906PC
Hermetic DIP	0°C to +70°C	AM2906DC
Dice	0°C to +70°C	AM2906XC
Hermetic DIP	−55°C to +125°C	AM2906DM
Hermetic Flat Pak	−55°C to +125°C	AM2906FM
Dice	−55°C to +125°C	AM2906XM

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs (Except Bus)	30mA
DC Output Current, Into Bus	200mA
DC Input Current	−30mA to +5.0mA

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

Am2906XC	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5%(COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am2906XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%(MIL)	MIN. = 4.50V	MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	MIL	I_{OL} = 40mA			0.5	Volts
				I_{OL} = 70mA			0.8	
				I_{OL} = 100mA			1.0	
			COM'L	I_{OL} = 40mA			0.5	
				I_{OL} = 70mA			0.7	
				I_{OL} =100mA			0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4V				−50	µA
			V_O = 4.5V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power OFF)	V_O = 4.5V					100	µA
V_{TH}	Receiver Input HIGH Threshold	Bus enable = 2.4V			2.3	2.0		Volts
V_{TL}	Receiver Input LOW Threshold	Bus enable = 2.4V				2.0	1.7	Volts

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2906XC	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$ (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am2906XM	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$ (MIL)	MIN. = 4.5V	MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL	$I_{OH} = -1mA$	2.4	3.4		Volts
			COM'L	$I_{OH} = -2.6mA$	2.4	3.4		
	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu A$, $V_{IN} = V_{IH}$ or V_{IL}		MIL	2.5	3.4		
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}		$I_{OL} = 4mA$			0.4	Volts
				$I_{OL} = 8mA$			0.45	
				$I_{OL} = 12mA$			0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4V$					−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7V$					20	µA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 5.5V$					100	µA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.		MIL	−6.0		−40	mA
				COM'L	−5.0		−42	
I_{CC}	Power Supply Current	V_{CC} = MAX., All inputs = GND				72		mA

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS ($T_A = +25°C$) — PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L(BUS) = 50pF, R_L(BUS) = 50Ω		21		ns
t_{PLH}				21		
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13		ns
t_{PLH}				13		
t_s	Data Inputs (A or B)	C_L = 15pF, R_L = 2kΩ	20			ns
t_h			5.0			
t_s	Select Inputs (S)		30			ns
t_h			5.0			
t_{PW}	Clock Pulse Width (HIGH)		20			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			17		ns
t_{PHL}				17		
t_{PLH}	Latch Enable to Receiver Output			15		ns
t_{PHL}				15		
t_s	Bus to Latch Enable ($\overline{RLE}$)		15			ns
t_h			0			
t_{PLH}	A or B Data to Odd Parity Output (Driver Enabled)			16		ns
t_{PHL}				16		
t_{PLH}	Bus to Odd Parity Output (Driver Inhibited, Latch Enabled)			18		ns
t_{PHL}				18		
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			16		ns
t_{PHL}				16		

FUNCTION TABLE

INPUTS						INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
S	A_i	B_i	DRCP	$\overline{BE}$	$\overline{RLE}$	D_i	Q_i	B_i	R_i	
X	X	X	X	H	X	X	X	H	X	Driver output disable
X	X	X	X	H	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	X	X	H	L	X	H	H	L	
X	X	X	X	X	H	X	NC	X	X	Latch received data
L	L	X	↑	X	X	L	X	X	X	Load driver register
L	H	X	↑	X	X	H	X	X	X	
H	X	L	↑	X	X	L	X	X	X	
H	X	H	↑	X	X	H	X	X	X	
X	X	X	L	X	X	NC	X	X	X	No driver clock restrictions
X	X	X	H	X	X	NC	X	X	X	
X	X	X	X	L	X	L	X	H	X	Drive Bus
X	X	X	X	L	X	H	X	L	X	

H = HIGH
L = LOW
Z = HIGH Impedance
NC = No change
X = Don't care
↑ = LOW-to-HIGH transition
i = 0, 1, 2, 3

PARITY OUTPUT FUNCTION TABLE

S	$\overline{BE}$	ODD PARITY OUTPUT
L	L	$ODD = A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	L	$ODD = B_0 \oplus B_1 \oplus B_2 \oplus B_3$
X	H	$ODD = Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

DEFINITION OF FUNCTIONAL TERMS

A_0, A_1, A_2, A_3 The "A" word data input into the two input multiplexers of the driver register.

B_0, B_1, B_2, B_3 The "B" word data input into the two input multiplexers of the driver register.

S Select. When the select input is LOW, the A data word is applied to the driver register. When the select input is HIGH, the B word is applied to the driver register.

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is LOW, the four drivers are in the high impedance state.

BUS_0, BUS_1 BUS_2, BUS_3 The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

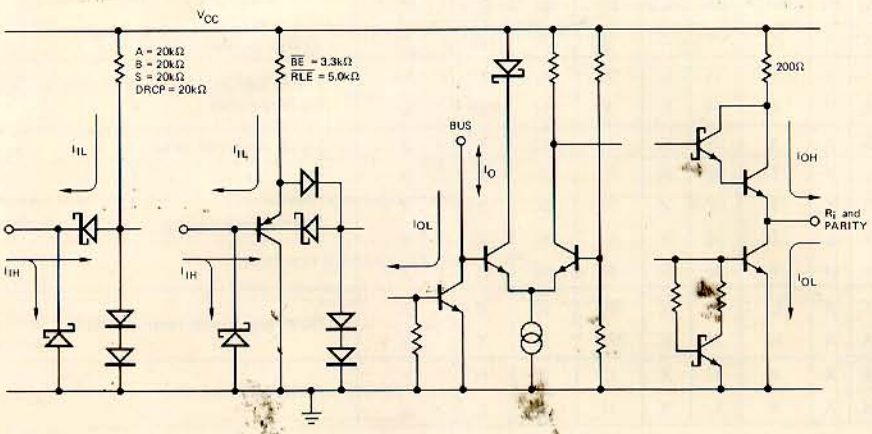
ODD Odd Parity Output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{RLE}$	1	1	–	–
R_0	2	–	50/130	33
B_0	3	1	–	–
A_0	4	1	–	–
BUS_0	5	–	OC	BUS
GND_1	6	–	–	–
BUS_1	7	–	OC	BUS
A_1	8	1	–	–
B_1	9	1	–	–
R_1	10	–	50/130	33
$\overline{BE}$	11	1	–	–
ODD	12	–	33	33
S	13	1	–	–
R_2	14	–	50/130	33
B_2	15	1	–	–
A_2	16	1	–	–
BUS_2	17	–	OC	BUS
GND_2	18	–	–	–
BUS_3	19	–	OC	BUS
A_3	20	1	–	–
B_3	21	1	–	–
R_3	22	–	50/130	33
DRCP	23	1	–	–
V_{CC}	24	–	–	–

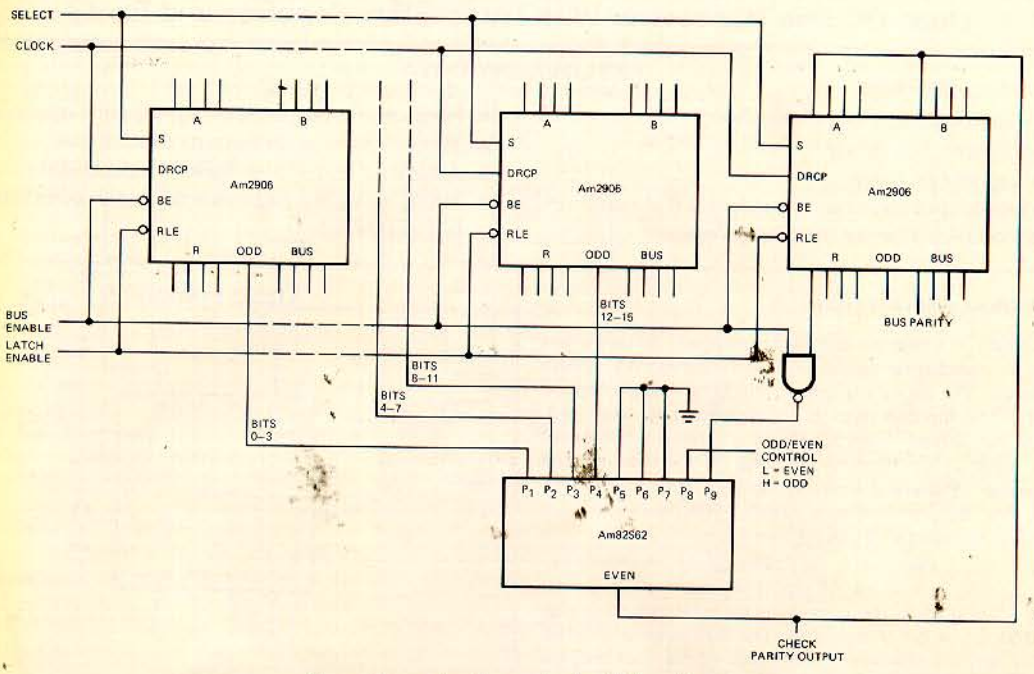
A Low Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

APPLICATIONS



Generating or checking parity for 16 data bits.

Am2907

Quad OC Bus Transceiver With Three-State Receiver and Parity

PRELIMINARY DATA

Distinctive Characteristics

- Quad high-speed LSI bus-transceiver
- Open-collector bus driver
- D-type register on driver
- Bus driver output can sink 100 mA at 0.8 V max.
- Internal odd 4-bit parity checker/generator
- Receiver has output latch for pipeline operation
- Three-state receiver outputs sink 12 mA
- Advanced Low-Power Schottky processing
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2907 is a high-performance, low-power Schottky bus transceiver intended for bipolar or MOS microprocessor system applications. The device consists of four D-type edge-triggered flip-flops. The flip-flop outputs are connected to four open-collector bus drivers. Each bus driver is internally connected to one input of a differential amplifier in the receiver. The four receiver differential amplifier outputs drive four D-type latches, that feature three-state outputs. The device also contains a four-bit odd parity checker/generator.

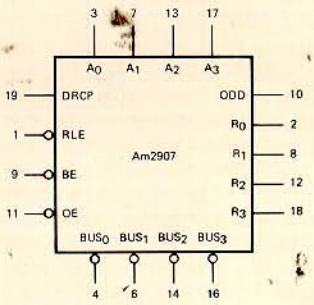
This LSI bus transceiver is fabricated using advanced low-power Schottky processing. All inputs (except the BUS inputs) are one LS unit load. The open-collector bus output can sink up to 100 mA at 0.8 V maximum. The BUS input differential amplifier contains disconnect protection diodes such that the bus is fail-safe when power is not applied. The bus enable input ($\overline{BE}$) is used to force the driver outputs to the high-impedance state. When $\overline{BE}$ is HIGH, the driver is disabled. The open-collector structure of the driver allows wired-OR operations to be performed on the bus.

The input register consists of four D-type flip-flops with a buffered common clock. The buffered common clock (DRCP) enters the A_i data into this driver register on the LOW-to-HIGH transition.

Data from the A input is inverted at the BUS output. Likewise, data at the BUS input is inverted at the receiver output. Thus, data is non-inverted from driver input to receiver output. The four receivers each feature a built-in D-type latch that is controlled from the buffered receiver latch enable ($\overline{RLE}$) input. When the $\overline{RLE}$ input is LOW, the latch is open and the receiver outputs will follow the bus inputs (BUS data inverted and $\overline{OE}$ LOW). When the $\overline{RLE}$ input is HIGH, the latch will close and retain the present data regardless of the bus input. The four latches have three-state outputs and are controlled by a buffered common three-state control ($\overline{OE}$) input. When $\overline{OE}$ is HIGH, the receiver outputs are in the high-impedance state.

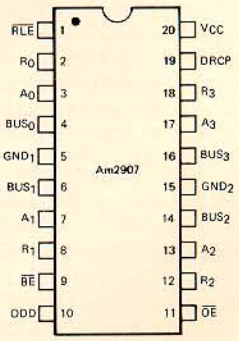
The Am2907 features a built-in four-bit odd parity checker/generator. The bus enable input ($\overline{BE}$) controls whether the parity output is in the generate or check mode. When the bus enable is LOW (driver enabled), odd parity is generated based on the A field data input to the driver register. When $\overline{BE}$ is HIGH, the parity output is determined by the four latch outputs of the receiver. Thus, if the driver is enabled, parity is generated and if the driver is in the high-impedance state, the BUS parity is checked.

LOGIC SYMBOL



V_{CC} = Pin 20
GND_1 = Pin 5
GND_2 = Pin 15

CONNECTION DIAGRAM
Top View

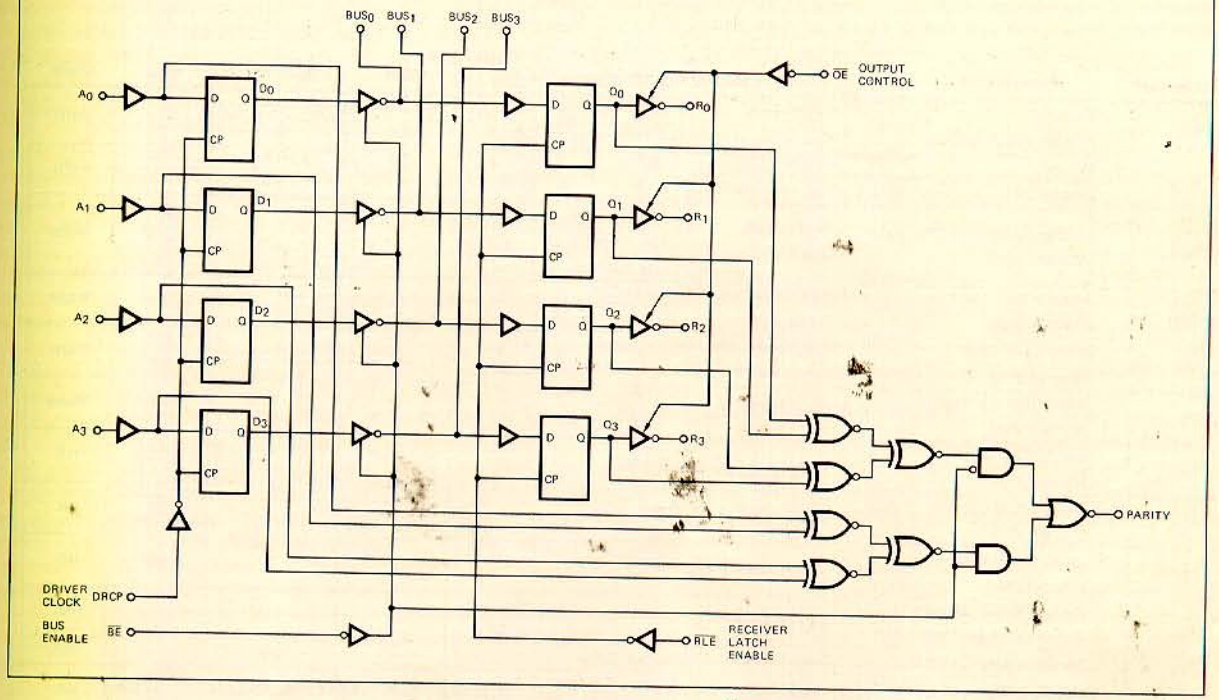


Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2907PC
Hermetic DIP	0°C to +70°C	AM2907DC
Dice	0°C to +70°C	AM2907XC
Hermetic DIP	−55°C to +125°C	AM2907DM
Hermetic Flat Pak	−55°C to +125°C	AM2907FM
Dice	−55°C to +125°C	AM2907XM

LOGIC DIAGRAM



MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs (Except BUS)	30 mA
DC Output Current, Into Bus	200 mA
DC Input Current	−30 mA to +5.0 mA

BUS INPUT/OUTPUT CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2907XC	T_A = 0°C to +70°C	V_{CC} = 5.0V ±5%(COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am2907XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ±10%(MIL)	MIN. = 4.50V	MAX. = 5.50V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OL}	Bus Output LOW Voltage	V_{CC} = MIN.	MIL	I_{OL} = 40mA			0.5	Volts
				I_{OL} = 70mA			0.8	
				I_{OL} = 100mA			1.0	
			COM'L	I_{OL} = 40mA			0.5	
				I_{OL} = 70mA			0.7	
				I_{OL} = 100mA			0.8	
I_O	Bus Leakage Current	V_{CC} = MAX.	V_O = 0.4 V				−50	µA
			V_O = 4.5 V	MIL			200	
				COM'L			100	
I_{OFF}	Bus Leakage Current (Power Off)	V_O = 4.5 V					100	µA
V_{TH}	Receiver Input HIGH Threshold	Bus Enable = 2.4 V			2.3	2.0		Volts
V_{TL}	Receiver Input LOW Threshold	Bus Enable = 2.4 V				2.0	1.7	Volts

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2907XC	$T_A = 0°C$ to $+70°C$	$V_{CC} = 5.0V \pm 5\%$ (COM'L)	MIN. = 4.75 V	MAX. = 5.25 V
Am2907XM	$T_A = -55°C$ to $+125°C$	$V_{CC} = 5.0V \pm 10\%$ (MIL)	MIN. = 4.50 V	MAX. = 5.50 V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Receiver Output HIGH Voltage	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	MIL: $I_{OH} = -1mA$		2.4	3.4		Volts
			COM'L: $I_{OH} = -2.6mA$		2.4	3.4		
V_{OH}	Parity Output HIGH Voltage	V_{CC} = MIN., $I_{OH} = -660\mu A$, $V_{IN} = V_{IH}$ or V_{IL}		MIL	2.5	3.4		Volts
				COM'L	2.7	3.4		
V_{OL}	Output LOW Voltage (Except Bus)	V_{CC} = MIN., $V_{IN} = V_{IL}$ or V_{IH}	I_{OL} = 4mA				0.4	Volts
			I_{OL} = 8mA				0.45	
			I_{OL} = 12mA				0.5	
V_{IH}	Input HIGH Level (Except Bus)	Guaranteed input logical HIGH for all inputs			2.0			Volts
V_{IL}	Input LOW Level (Except Bus)	Guaranteed input logical LOW for all inputs		MIL			0.7	Volts
				COM'L			0.8	
V_I	Input Clamp Voltage (Except Bus)	V_{CC} = MIN., $I_{IN} = -18mA$					−1.5	Volts
I_{IL}	Input LOW Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 0.4$ V					−0.36	mA
I_{IH}	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 2.7$ V					20	μA
I_I	Input HIGH Current (Except Bus)	V_{CC} = MAX., $V_{IN} = 5.5$ V					100	μA
I_{SC}	Output Short Circuit Current (Except Bus)	V_{CC} = MAX.		MIL	−6		−40	mA
				COM'L	−5		−42	
I_{CC}	Power Supply Current	V_{CC} = MAX., All Inputs = GND				69		mA
I_O	Off-State Output Current (Receiver Outputs)	V_{CC} = MAX.	$V_O = 2.4$ V				20	μA
			$V_O = 0.4$ V				−20	

Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at $V_{CC} = 5.0V$, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

SWITCHING CHARACTERISTICS ($T_A = +25°C$) — PRELIMINARY DATA

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PHL}	Driver Clock (DRCP) to Bus	C_L (BUS) = 50pF, R_L (BUS) = 50Ω		21		ns
t_{PLH}				21		
t_{PHL}	Bus Enable ($\overline{BE}$) to Bus			13		ns
t_{PLH}				13		
t_s	A Data Inputs	C_L = 15pF, R_L = 2kΩ	20			ns
t_h			5			
t_{pw}	Clock Pulse Width (HIGH)		20			ns
t_{PLH}	Bus to Receiver Output (Latch Enabled)			17		ns
t_{PHL}				17		
t_{PLH}	Latch Enable to Receiver Output			15		ns
t_{PHL}				15		
t_s	Bus to Latch Enable ($\overline{RLE}$)		15			ns
t_h			0			
t_{PLH}	A Data to Odd Parity Out (Driver Enabled)			16		ns
t_{PHL}				16		
t_{PLH}	Bus to Odd Parity Out (Driver Inhibited)			18		ns
t_{PHL}				18		
t_{PLH}	Latch Enable ($\overline{RLE}$) to Odd Parity Output			16		ns
t_{PHL}				16		
t_{ZH}	Output Control to Output	C_L = 15pF, R_L = 2kΩ		10		ns
t_{ZL}				14		
t_{HZ}	Output Control to Output			10		ns
t_{LZ}				9		

TRUTH TABLE

INPUTS					INTERNAL TO DEVICE		BUS	OUTPUT	FUNCTION
A_i	DRCP	$\overline{BE}$	$\overline{RLE}$	$\overline{OE}$	D_i	Q_i	B_i	R_i	
X	X	H	X	X	X	X	H	X	Driver output disable
X	X	X	X	H	X	X	X	Z	Receiver output disable
X	X	H	L	L	X	L	L	H	Driver output disable and receive data via Bus input
X	X	H	L	L	X	H	H	L	
X	X	X	H	X	X	NC	X	X	Latch received data
L	↑	X	X	X	L	X	X	X	Load driver register
H	↑	X	X	X	H	X	X	X	
X	L	X	X	X	NC	X	X	X	No driver clock restrictions
X	H	X	X	X	NC	X	X	X	
X	X	L	X	X	L	X	H	X	Drive Bus
X	X	L	X	X	H	X	L	X	

H = HIGH Z = High Impedance X = Don't Care i = 0, 1, 2, 3
L = LOW NC = No Change ↑ = LOW-to-HIGH Transition

PARITY OUTPUT FUNCTION TABLE

$\overline{BE}$	ODD PARITY OUTPUT
L	ODD = $A_0 \oplus A_1 \oplus A_2 \oplus A_3$
H	ODD = $Q_0 \oplus Q_1 \oplus Q_2 \oplus Q_3$

DEFINITION OF FUNCTIONAL TERMS

DRCP Driver Clock Pulse. Clock pulse for the driver register.

$\overline{BE}$ Bus Enable. When the Bus Enable is LOW, the four drivers are in the high impedance state.

BUS_0, BUS_1, BUS_2, BUS_3 The four driver outputs and receiver inputs (data is inverted).

R_0, R_1, R_2, R_3 The four receiver outputs. Data from the bus is inverted while data from the A or B inputs is non-inverted.

$\overline{RLE}$ Receiver Latch Enable. When $\overline{RLE}$ is LOW, data on the BUS inputs is passed through the receiver latches. When $\overline{RLE}$ is HIGH, the receiver latches are closed and will retain the data independent of all other inputs.

ODD Odd parity output. Generates parity with the driver enabled, checks parity with the driver in the high-impedance state.

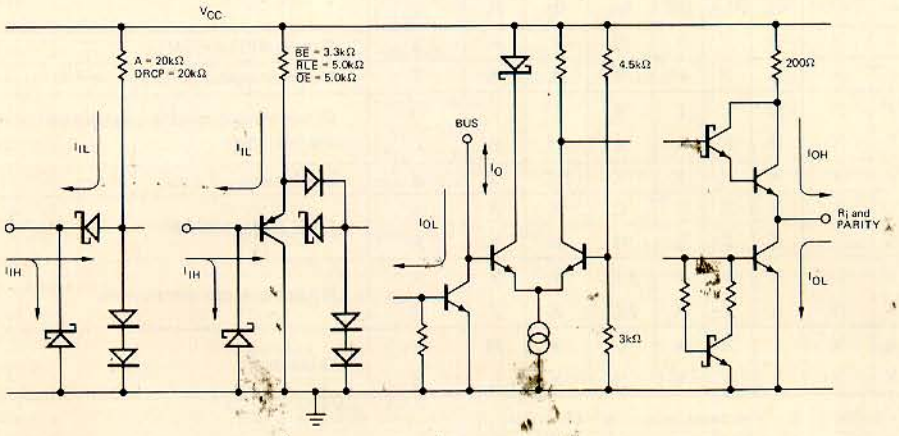
$\overline{OE}$ Output Enable. When the $\overline{OE}$ input is HIGH, the four three-state receiver outputs are in the high-impedance state.

LOADING RULES IN UNIT LOADS

Input/Output	Pin No's	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
$\overline{RLE}$	1	1	–	–
R_0	2	–	50/130	33
A_0	3	1	–	–
BUS_0	4	–	OC	BUS
GND_1	5	–	–	–
BUS_1	6	–	OC	BUS
A_1	7	1	–	–
R_1	8	–	50/130	33
$\overline{BE}$	9	1	–	–
ODD	10	–	33	33
$\overline{OE}$	11	1	–	–
R_2	12	–	50/130	33
A_2	13	1	–	–
BUS_2	14	–	OC	BUS
GND_2	15	–	–	–
BUS_3	16	–	OC	BUS
A_3	17	1	–	–
R_3	18	–	50/130	33
DRCP	19	1	–	–
V_{CC}	20	–	–	–

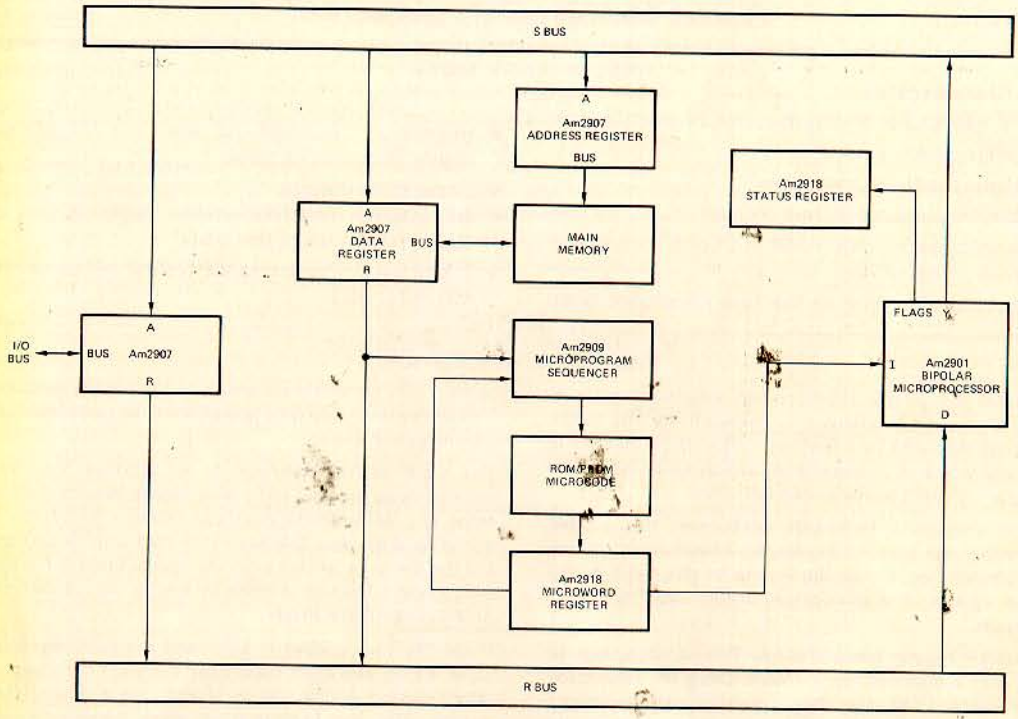
A Low Power Schottky TTL Unit Load is defined as 20μA measured at 2.7V HIGH and −0.36mA measured at 0.4V LOW.

INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

APPLICATIONS



The Am2907 can be used as an I/O Bus Transceiver and Main Memory I/O Transceiver in high-speed Microprocessor Systems.

Am2909

Bipolar Microprogram Sequencer

PRELIMINARY DATA

Distinctive Characteristics

- 4-bit slice cascadable to any number of microwords
- Internal instruction register
- Branch input for N-way branches
- Cascadable 4-bit microprogram counter
- 4 x 4 file with stack pointer and push pop control for nesting microsubroutines.
- Zero input for returning to the zero microcode word
- Individual OR input for each bit for branching to higher microinstructions
- Three-state outputs
- All internal registers change state on the LOW-to-HIGH transition of the clock
- 100% reliability assurance testing in compliance with MIL-STD-883

FUNCTIONAL DESCRIPTION

The Am2909 is a bipolar microprogram sequencer intended for use in high-speed microprocessor applications. The device is a cascadable 4-bit slice such that two devices allow addressing of up to 256-words of microprogram and three devices allow addressing of up to 4K words of microprogram.

The device contains a four-input multiplexer that is used to select either the instruction register, branch input, microprogram counter, or file as the source of the next microinstruction address. This multiplexer is controlled by the S_0 and S_1 inputs.

The instruction register consists of four D-type, edge-triggered flip-flops with a common clock enable. When the instruction register enable is LOW, new data is entered into the register on the clock LOW-to-HIGH transition. The instruction register is available at the multiplexer as a source for the next microinstruction address. Likewise, the branch input is a four-bit field of direct inputs to the multiplexer and can be selected as the next microinstruction address. This allows an N-way branch where N is any word in the microcode.

The Am2909 contains a microprogram counter (μPC) that is composed of a 4-bit incrementer followed by a 4-bit register. The incrementer has carry-in (C_n) and carry-out (C_{n+4}) such that cascading to larger word lengths is straight-forward. The μPC can be used in either of two ways. When the least significant carry-in to the incrementer is HIGH, the microprogram register is loaded on the next clock cycle with the current Y output word plus one (PC ← Y+1). Thus sequential microinstructions can be executed. If this least significant C_n is LOW, the incrementer passes the Y output word unmodified and the microprogram register is loaded with the same Y word on the next clock cycle (PC←Y). Thus, the same microinstruction can be executed any number of times by using the least significant C_n as the control.

The last input available at the multiplexer input is the 4 x 4 file (stack). The file is used to provide return address linkage when executing microsubroutines. The file contains a built-in stack pointer (SP) which always points to the last file word written. This allows stack reference operations to be performed without causing a push or pop.

The stack pointer operates as an up/down counter with separate push/pop and file enable inputs. When the file enable input is LOW and the push/pop input is HIGH, the PUSH operation is enabled. This causes the stack pointer to increment and the file to be written with the required return linkage—the next microinstruction address following the subroutine jump which initiated the PUSH.

If the file enable input is LOW and the push/pop control is LOW, a POP operation occurs. This implies the usage of the return linkage during this cycle and thus a return from subroutine. The next LOW-to-HIGH clock transition causes the stack pointer to decrement. If the file enable is HIGH, no action is taken by the stack pointer, regardless of any other input.

The stack pointer linkage is such that any combination of pushes, pops or stack references can be achieved. Likewise, one microinstruction subroutines can be performed. Since the stack is 4 words deep, up to four microsubroutines can be nested.

The ZERO input is used to force the 4 outputs to the binary zero state. When the ZERO input is LOW, all Y outputs are LOW regardless of any other inputs (except $\overline{OE}$). Each Y output bit also has a separate OR input such that a conditional logic one can be forced at each Y output. This allows jumping to different microinstructions on programmed conditions.

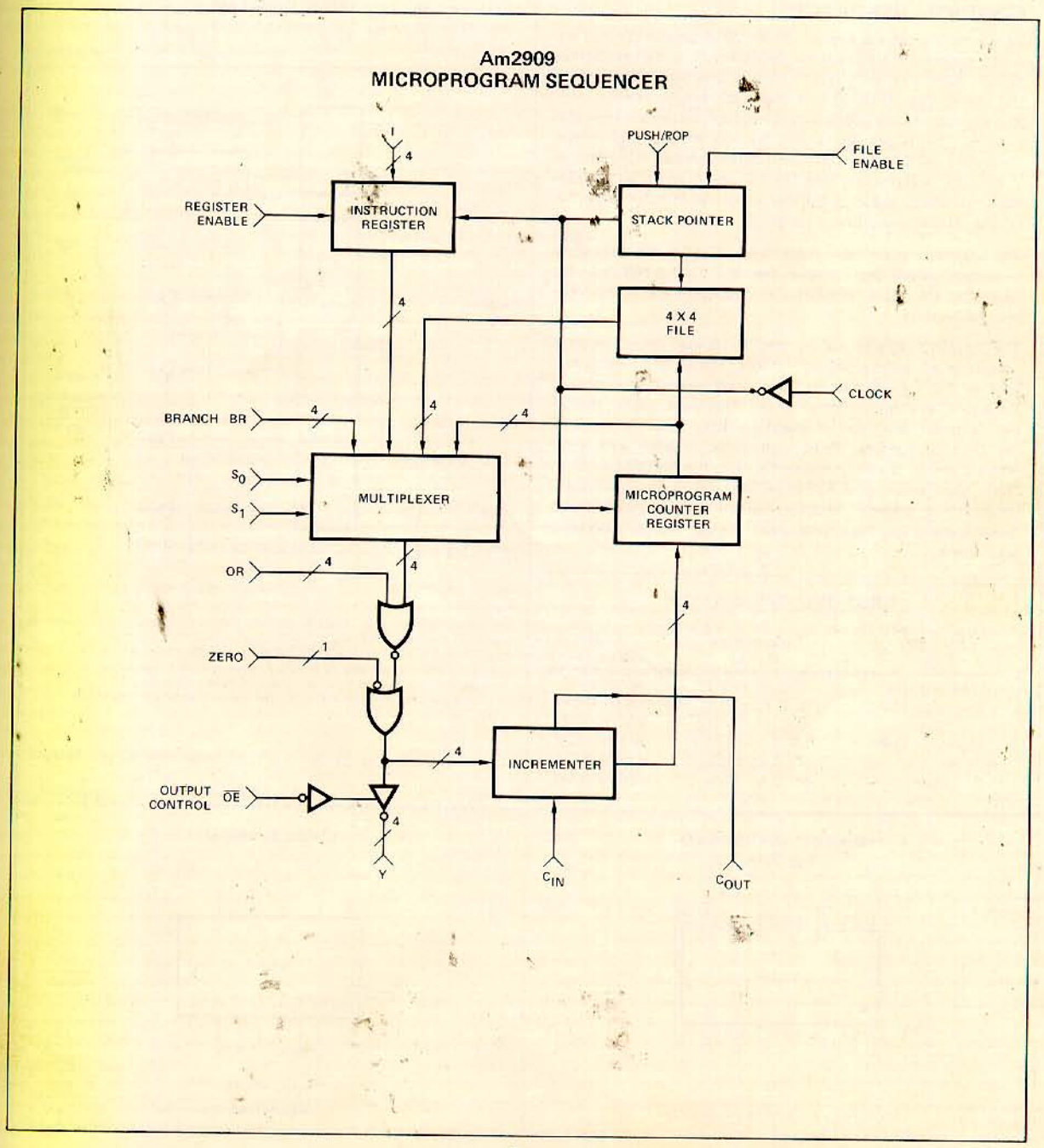
The Am2909 features three-state Y outputs. These can be particularly useful in military designs requiring external Ground Support Equipment (GSE) to provide automatic checkout of the microprocessor. The internal control can be placed in the high-impedance state, and preprogrammed sequences of microinstructions can be executed via external access to the control ROM/PROM.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Hermetic DIP	0°C to +70°C	AM2909DC
Dice	0°C to +70°C	AM2909XC
Hermetic DIP	−55°C to +125°C	AM2909DM
Dice	−55°C to +125°C	AM2909XM

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential	−0.5 V to +7 V
DC Voltage Applied to Outputs for HIGH Output State	−0.5 V to +V_{CC} max.
DC Input Voltage	−0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	−30 mA to +5.0 mA



Am2918

Quad D Register With Standard And Three-State Outputs

Distinctive Characteristics

- Advanced Schottky technology
- Four D-type flip-flops
- Four standard totem-pole outputs
- Four three-state outputs
- 75 MHz clock frequency
- 100% reliability assurance testing in compliance with MIL-STD-883

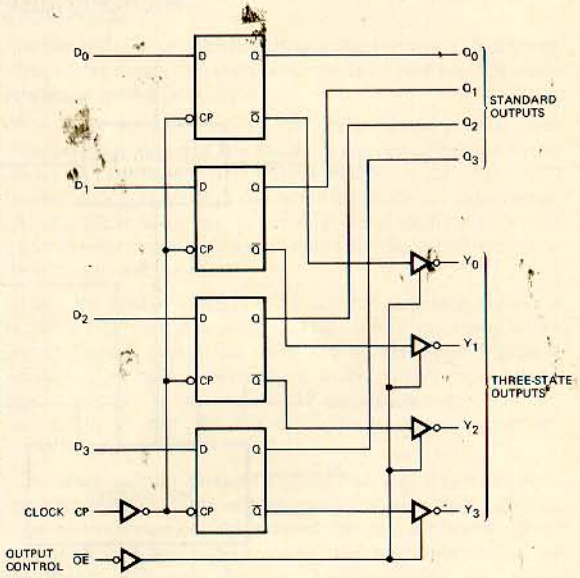
FUNCTIONAL DESCRIPTION

New Schottky circuits such as the Am2918 register provide the design engineer with additional flexibility in system configuration — especially with regard to bus structure, organization and speed. The Am2918 is a quadruple D-type register with four standard totem pole outputs and four three-state bus-type outputs. The 16-pin device also features a buffered common clock (CP) and a buffered common output control ($\overline{OE}$) for the Y outputs. Information meeting the set-up and hold requirements on the D inputs is transferred to the Q outputs on the LOW-to-HIGH transition of the clock.

The same data as on the Q outputs is enabled at the three-state Y outputs when the "output control" ($\overline{OE}$) input is LOW. When the $\overline{OE}$ input is HIGH, the Y outputs are in the high-impedance state.

The Am2918 register can be used in bipolar microprocessor designs as an address register, status register, instruction register or for various data or microword register applications. Because of the unique design of the three-state output, the device features very short propagation delay from the clock to the Q or Y outputs. Thus, system performance and architectural design can be improved by using the Am2918 register. Other applications of Am2918 register can be found in microprogrammed display systems, communication systems and most general or special purpose digital signal processing equipment.

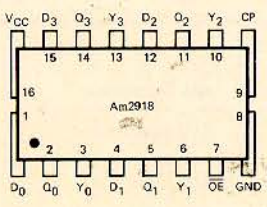
LOGIC DIAGRAM



ORDERING INFORMATION

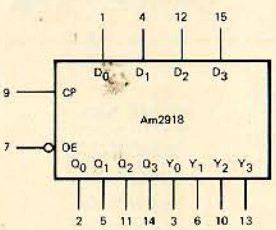
Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2918PC
Hermetic DIP	0°C to +70°C	AM2918DC
Dice	0°C to +70°C	AM2918XC
Hermetic DIP	−55°C to +125°C	AM2918DM
Hermetic Flat Pack	−55°C to +125°C	AM2918FM
Dice	−55°C to +125°C	AM2918XM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
Supply Voltage to Ground Potential (Pin 16 to Pin 8) Continuous	−0.5V to +7V
DC Voltage Applied to Outputs for HIGH Output State	−0.5V to +V_{CC} max.
DC Input Voltage	−0.5V to +5.5V
DC Output Current, Into Outputs	30mA
DC Input Current	−30mA to +5.0mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am2918XC	T_A = 0°C to +70°C	V_{CC} = 5.0V ± 5% (COM'L)	MIN. = 4.75V	MAX. = 5.25V
Am2918XM	T_A = −55°C to +125°C	V_{CC} = 5.0V ± 10% (MIL)	MIN. = 4.5V	MAX. = 5.5V

Parameters	Description	Test Conditions (Note 1)			Min.	Typ. (Note 2)	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Q	I_{OH} = −1mA MIL	2.5	3.4		Volts
				I_{OH} = −1mA COM'L	2.7	3.4		
			Y	XM, I_{OH} = −2mA	2.4	3.4		
				XC, I_{OH} = −6.5mA	2.4	3.4		
V_{OL}	Output LOW Voltage (Note 6)	V_{CC} = MIN., I_{OL} = 20mA, V_{IN} = V_{IH} or V_{IL}					0.5	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.2	Volts
I_{IL} (Note 3)	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V					−2.0	mA
I_{IH} (Note 3)	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V					50	µA
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_O	Y Output Off-State Leakage Current	V_{CC} = MAX.		V_O = 2.4V			50	µA
				V_O = 0.4V			−50	
I_{SC}	Output Short Circuit Current (Note 4)	V_{CC} = MAX.			−40		−100	mA
I_{CC}	Power Supply Current	V_{CC} = MAX. (Note 5)				80	130	mA

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, T_A = 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (see Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test shoud not exceed one second.
5. I_{CC} is measured with all inputs at 4.5V and all outputs open.
6. Measured on Q outputs with Y outputs open. Measured on Y outputs with Q outputs open.

Switching Characteristics (T_A = +25°C, V_{CC} = 5.0V, R_L = 280Ω) For additional information, see pages 126 and 127.

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t_{PLH}	Clock to Q Output	C_L = 15pF		6.0	9.0	ns
t_{PHL}				8.5	13	
t_{pw}	Clock Pulse Width		7.0			ns
t_s	Data		5.0			ns
t_h	Data		3.0			ns
t_{PLH}	Clock to Y Output ($\overline{OE}$ LOW)			6.0	9.0	ns
t_{PHL}				8.5	13	
t_{ZH}	Output Control to Output	C_L = 5pF		12.5	19	ns
t_{ZL}				12	18	
t_{HZ}		C_L = 50pF		4.0	6.0	
t_{LZ}				7.0	10.5	
f_{max}	Maximum Clock Frequency	C_L = 15pF	75	100		MHz

TRUTH TABLE

INPUTS			OUTPUTS		NOTES
$\overline{OE}$	CLOCK CP	D	Q	Y	
H	L	X	NC	Z	–
H	H	X	NC	Z	–
H	↑	L	L	Z	–
H	↑	H	H	Z	–
L	↑	L	L	L	–
L	↑	H	H	H	–
L	–	–	L	L	1
L	–	–	H	H	1

L = LOW
H = HIGH
X = Don't care

NC = No change
↑ = LOW to HIGH transition
Z = High impedance

Note: 1. When $\overline{OE}$ is LOW, the Y output will be in the same logic state as the Q output.

DEFINITION OF FUNCTIONAL TERMS

D_i The four data inputs to the register.

Q_i The four data outputs of the register with standard totem-pole active pull-up outputs. Data is passed non-inverted.

Y_i The four three-state data outputs of the register. When the three-state outputs are enabled, data is passed non-inverted. A HIGH on the "output control" input forces the Y_i outputs to the high-impedance state.

CP Clock. The buffered common clock for the register. Enters data on the LOW-to-HIGH transition.

$\overline{OE}$ Output Control. When the $\overline{OE}$ input is HIGH, the Yi outputs are in the high-impedance state. When the $\overline{OE}$ input is LOW, the TRUE register data is present at the Y_i outputs.

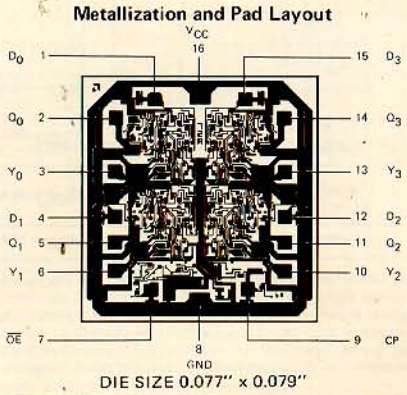
LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out Output HIGH	Fan-out Output LOW
D_0	1	1	–	–
Q_0	2	–	20	10*
Y_0	3	–	40/130	10*
D_1	4	1	–	–
Q_1	5	–	20	10*
Y_1	6	–	40/130	10*
$\overline{OE}$	7	1	–	–
GND	8	–	–	–
CP	9	1	–	–
Y_2	10	–	40/130	10*
Q_2	11	–	20	10*
D_2	12	1	–	–
Y_3	13	–	40/130	10*
Q_3	14	–	20	10*
D_3	15	1	–	–
V_{CC}	16	–	–	–

A Schottky TTL Unit Load is defined as 50μA measured at 2.7V HIGH and −2.0mA measured at 0.5V LOW.

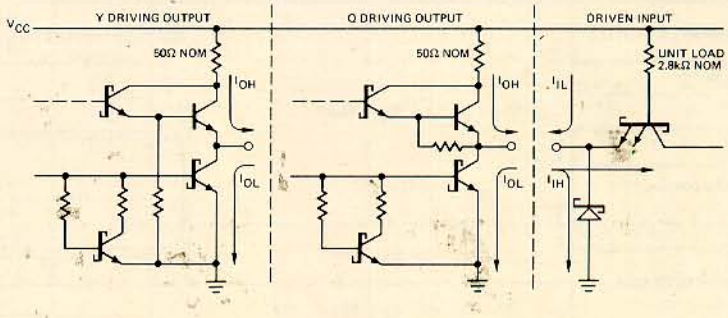
*Fan-out on each Q_i and Y_i output pair should not exceed 15 unit loads (30mA) for i = 0, 1, 2, 3.

Metallization and Pad Layout



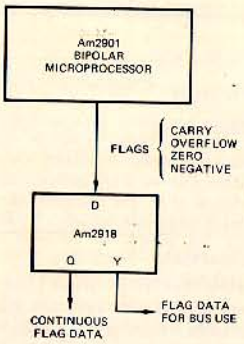
DIE SIZE 0.077" x 0.079"

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS

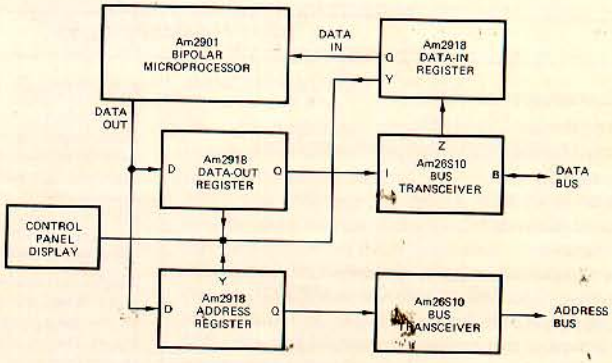


Note: Actual current flow direction shown.

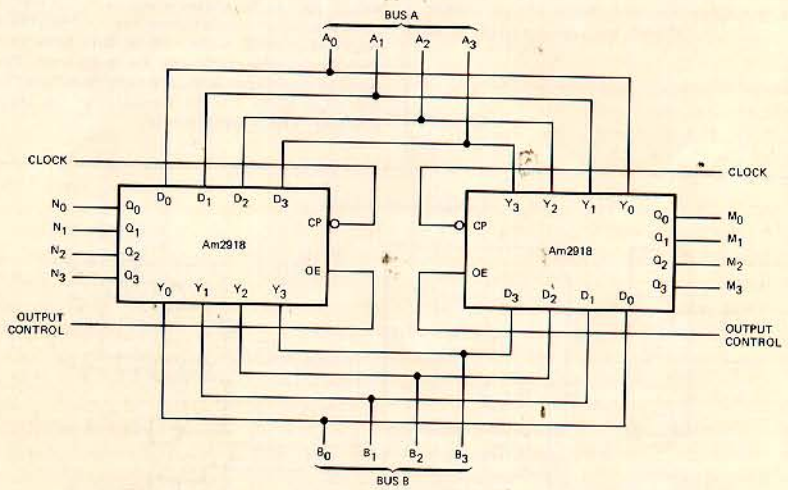
APPLICATIONS



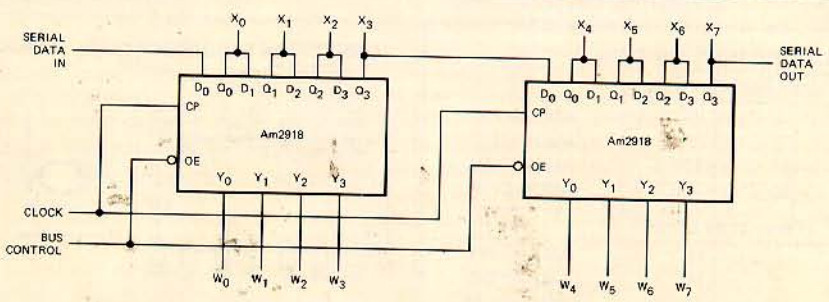
The Am2918 as a 4-Bit status register



The Am2918 used as data-in, data-out and address registers.



The Am25S18 can be connected for bi-directional interface between two buses. The device on the left stores data from the A-bus and drives the A-bus. The device on the right stores data from the B-bus and drives the A-bus. The output control is used to place either or both drivers in the high-impedance state. The contents of each register are available for continuous usage at the N and M ports of the device.



8-Bit serial to parallel converter with three-state output (W) and direct access to the register word (X).

Am2950/Am2951

256-Bit Random Access Memories

PRELIMINARY DATA

Distinctive Characteristics

- Fully decoded 256-bit TTL RAMs.
- Open collector (Am2950) and three-state (Am2951)
- High speed operation:
  35ns typical access time
- Very low power dissipation
  275mW typical
- Full military temperature range performance.
  100% tested to GALPAT at −55°C and +125°C
  10% power supply tolerance
- Low-power Schottky processing with internal ECL circuitry
  Uniform access times over voltage and temperature variations.
- Tested to GALPAT.
  Functional and switching characteristics are guaranteed for all data and address patterns.

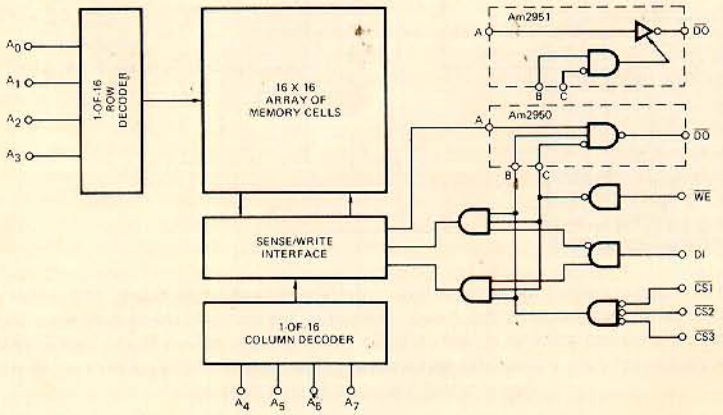
FUNCTIONAL DESCRIPTION

The Am2950 and Am2951 are fully decoded bipolar random access memories for use in high-speed buffer memories and as a replacement for high-speed core memories in digital systems. The memories are organized 256-words by 1-bit with an 8-bit binary address field and separate data in and data output lines. The memories have three active LOW chip select inputs and a three-state output (Am2951) or open-collector output (Am2950). All inputs are buffered to present an input load of only 0.5 TTL unit loads.

Read/write operation is controlled by an active LOW write enable input. When the write enable is LOW and the chip is selected the data on the data input is written into the location specified by the address inputs. During this operation the output floats allowing the data bus to be used by other memories or open-collector logic elements that are tied to the inverting data output. Reading is accomplished by having the chip selected and the write enable input HIGH. Data stored in the location specified by the address inputs is read out and appears on the data output inverted.

The chip is selected by three active LOW inputs all of which must be LOW in order for the data output to be active during the read operation and for data to be written into or from the memory. These three active LOW chip select inputs permit the Am25LS138 MSI decoder to select memories in either a one, two or three dimensionsl mode of operation when large memory systems are being built. The delay from the chip select to the output is considerably faster than from the address inputs and extra delay can be tolerated in the chip select path without affecting system performance.

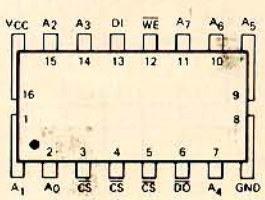
LOGIC DIAGRAM



ORDERING INFORMATION

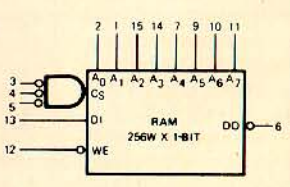
Open Collector Output		
Molded DIP	0°C to +75°C	AM2950PC
Hermetic DIP	0°C to +75°C	AM2950DC
Hermetic DIP	−55°C to +125°C	AM2950DM
Flat Pack	−55°C to +125°C	AM2950FM
Three State Output		
Molded DIP	0°C to +75°C	AM2951PC
Hermetic DIP	0°C to +75°C	AM2951DC
Hermetic DIP	−55°C to +125°C	AM2951DM
Flat Pack	−55°C to +125°C	AM2951FM

CONNECTION DIAGRAM
Top View



Note: Pin 1 is marked for orientation.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

Am2952

High-Speed 1024-Bit Random Access Memories

PRELIMINARY DATA

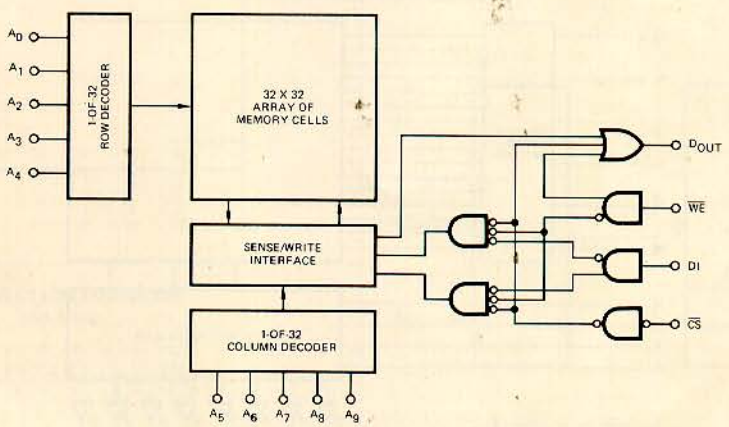
Distinctive Characteristics

- Fully decoded 1024 x 1 bipolar RAMs
- High speed operation:
  30ns typical access time
- Low input loading
  Easy expansion without extra buffers
- Output is OFF during write pulse, reduced noise. Input and output can be tied to common bus.
- Internal ECL circuitry
  Uniform access times over voltage and temperature variations.
- Tested with scan, read-modify-write, and address complement patterns.
  Functional and switching characteristics are guaranteed for all data and address patterns.

FUNCTIONAL DESCRIPTION

The Am2952 is a 1024-word by 1-bit bipolar read-write memory for use in high-speed memory systems. Reading and writing are under control of an active LOW chip select ($\overline{CS}$). When the chip select is HIGH, the output is OFF, and the voltage level on the output will be determined by external components. When the chip select is LOW, reading and writing can occur. The mode is selected by the active LOW write enable ($\overline{WE}$). When it is HIGH, the data bit addressed by the ten address lines A_0–A_9 is read out on the data output. The output will go LOW if a logic LOW level were stored, and will remain OFF if a logic HIGH level were stored. Writing is performed when the write enable is LOW. Data on the data input (D_{IN}) is written into the addressed location. The memory is non-inverting: a LOW level written in appears as a LOW level read out. The output turns OFF while the write enable is LOW. An external pull-up resistor should be connected to the open collector output to establish a logic HIGH level when the output is OFF.

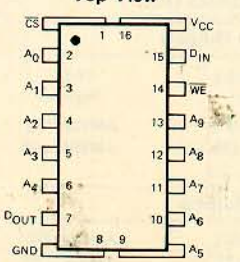
LOGIC DIAGRAM



ORDERING INFORMATION

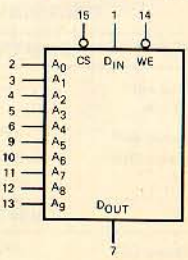
Package Type	Temperature Range	Order Number
Molded DIP	0°C to +70°C	AM2952PC
Hermetic DIP	0°C to +70°C	AM2952DC
Hermetic DIP	–55°C to +125°C	AM2952DM
Hermetic Flat Pak	–55°C to +125°C	AM2952FM

CONNECTION DIAGRAM
Top View



Note:
Pin 1 is marked for orientation.

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

Am2960/Am2961

1024-Word by 8-Bit Read Only Memories

PRELIMINARY DATA

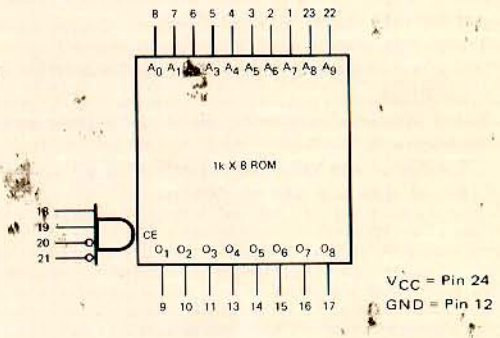
Distinctive Characteristics

- Fully decoded 8192-bit mask programmable ROM
- Access time 100 ns typical
- Available with three-state outputs (Am2961) or with open collector outputs (Am2960)
- Pin compatible with 8k PROM's
- 100% reliability assurance testing in compliance with MIL-STD-883

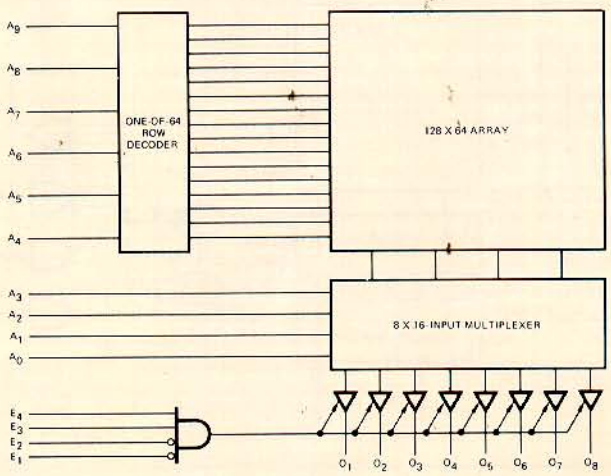
FUNCTIONAL DESCRIPTION

The Am2960 and Am2961 are 8192-bit mask programmable Read Only Memories organized as 1024 words by 8 bits. Data is permanently stored in the device by use of a special metallization pattern, generated to correspond to the customer's data pattern. Each device has four chip enable inputs, two of which are active HIGH and two of which are active LOW. Data appears on the output when all four chip enable inputs are active. If any chip enable input is not active the outputs will be in a high-impedance OFF state. The Am2961 has three-state outputs, so an enabled chip will have outputs in standard TTL HIGH or LOW states. The Am2960 has open collector outputs, so the HIGH level must be established by external pull-up resistors.

LOGICAL SYMBOL



LOGIC BLOCK DIAGRAM



ORDERING INFORMATION

Open Collector Outputs

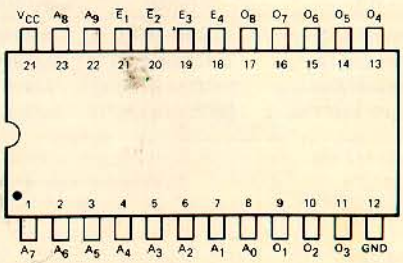
Package Type	Temperature Range	Order Number
Hermetic DIP	0°C to +75°C	AM2960DC
Hermetic DIP	−55°C to +125°C	AM2960DM

Three-State Outputs

Package Type	Temperature Range	Order Number
Hermetic DIP	0°C to +75°C	AM2961DC
Hermetic DIP	−55°C to +125°C	AM2961DM

CONNECTION DIAGRAM

Top View



Note: Pin 1 is marked for orientation.

Am2970/Am2971

256-Word by 4-Bit PROMS

PRELIMINARY DATA

Distinctive Characteristics

- Field programmable read only memory
- Highly reliable polysilicon fuses
- Pin compatible with other popular 256 by 4 PROMS
- Typical fusing time of 200μs/bit
- 60ns access time
- Three-state and open-collector versions

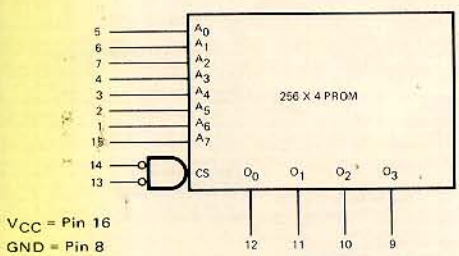
FUNCTIONAL DESCRIPTION

The Am2970 and Am2971 are electrically programmable Schottky TTL read only memories. Both devices are organized as 256 words of 4 bits each; the Am2970 has open collector outputs and the Am2971 has three-state outputs. The devices are shipped with all bits HIGH and each bit in the memory can be programmed to a LOW by applying appropriate voltages to the circuit. At each bit location on the circuit there is a narrow link of polysilicon material which is conductive, but which can be opened like a fuse by passing a short, high-current pulse through it. The fusing process simply melts the polysilicon at the center of the link and the two melted ends pull away from each other insuring a very reliable open circuit, which produces a LOW at the memory output.

The programming voltage is applied at the output pin for the bit to be programmed, while the word to be programmed is selected by normal TTL levels on the address lines. The passage of current through the link is controlled by a programming pulse on the chip select input. There are two extra words and one additional bit for each word on the chip which are programmed at the factory during testing to insure high programming yields in devices shipped.

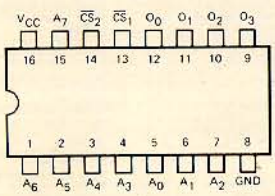
After programming, the device can be used for microprogram storage or random logic function generation, like any read-only memory. If either chip select input is held HIGH, the outputs will all turn off, so the outputs of several memories can be tied together for expansion.

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
Top View

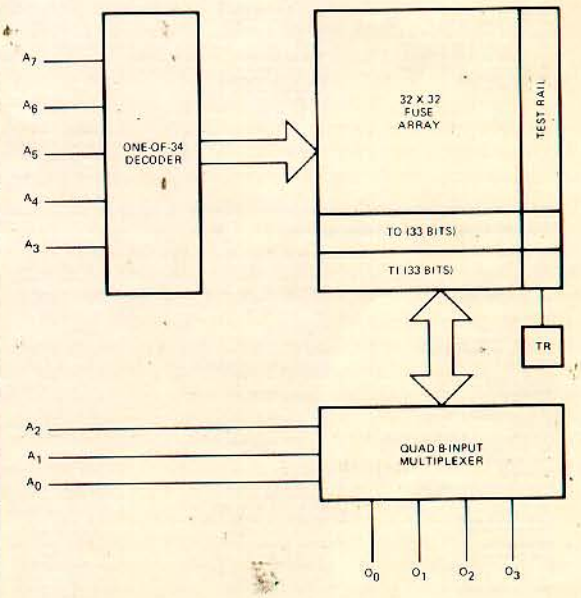


Note: Pin 1 is marked for orientation.

ORDERING INFORMATION

Package Type	Temperature Range	Order Number
Open Collectors		
Hermetic DIP	0°C to +75°C	AM2970DC
Hermetic DIP	−55°C to +125°C	AM2970DM
Three-State Outputs		
Hermetic DIP	0°C to +75°C	AM2971DC
Hermetic DIP	−55°C to +125°C	AM2971DM

BLOCK DIAGRAM



TO = Test Word
TI = Test Word
TR = Test Rail

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